Fig. 1A

Prior Art

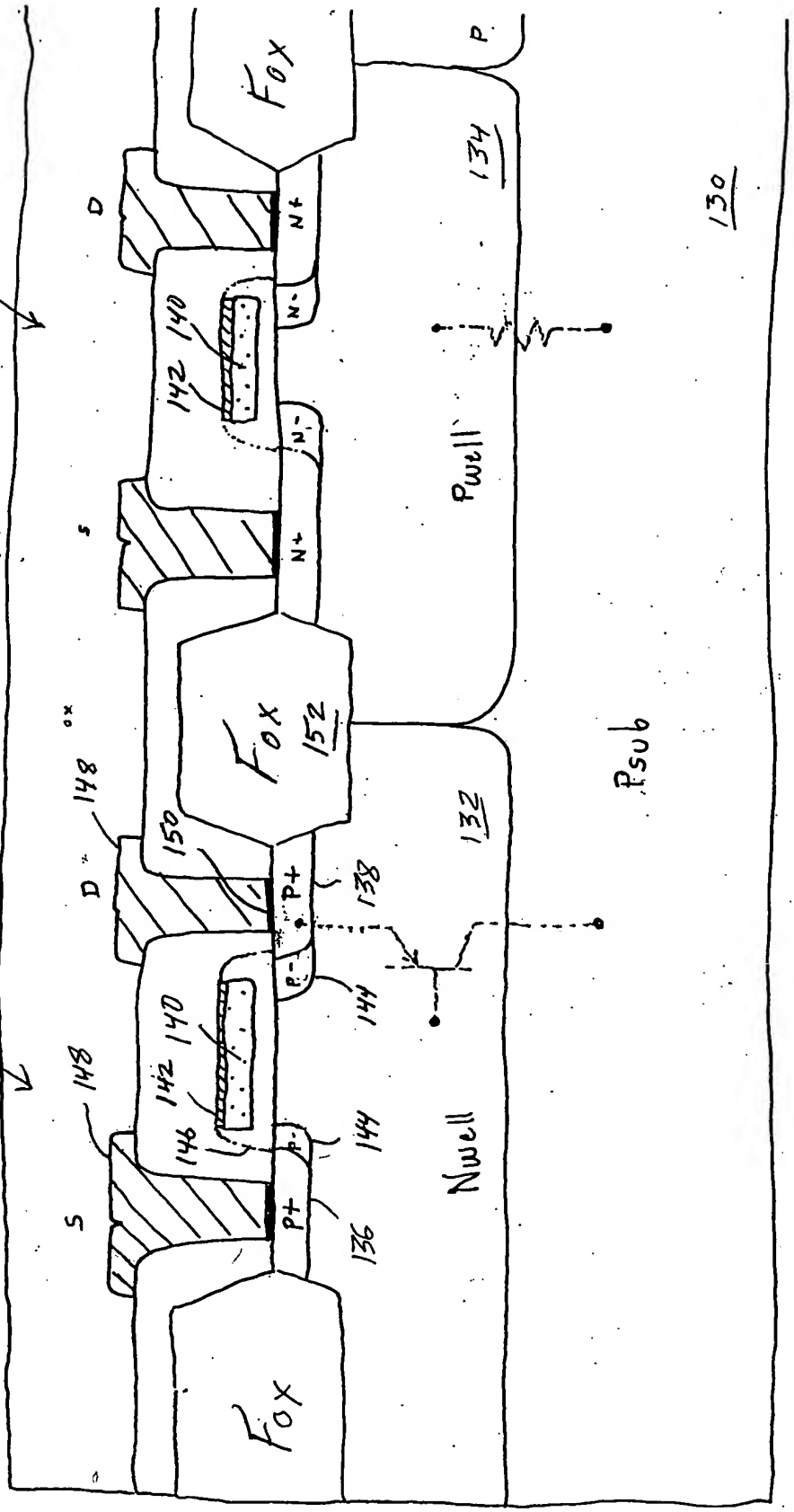


Fig. 1C
Prior Art

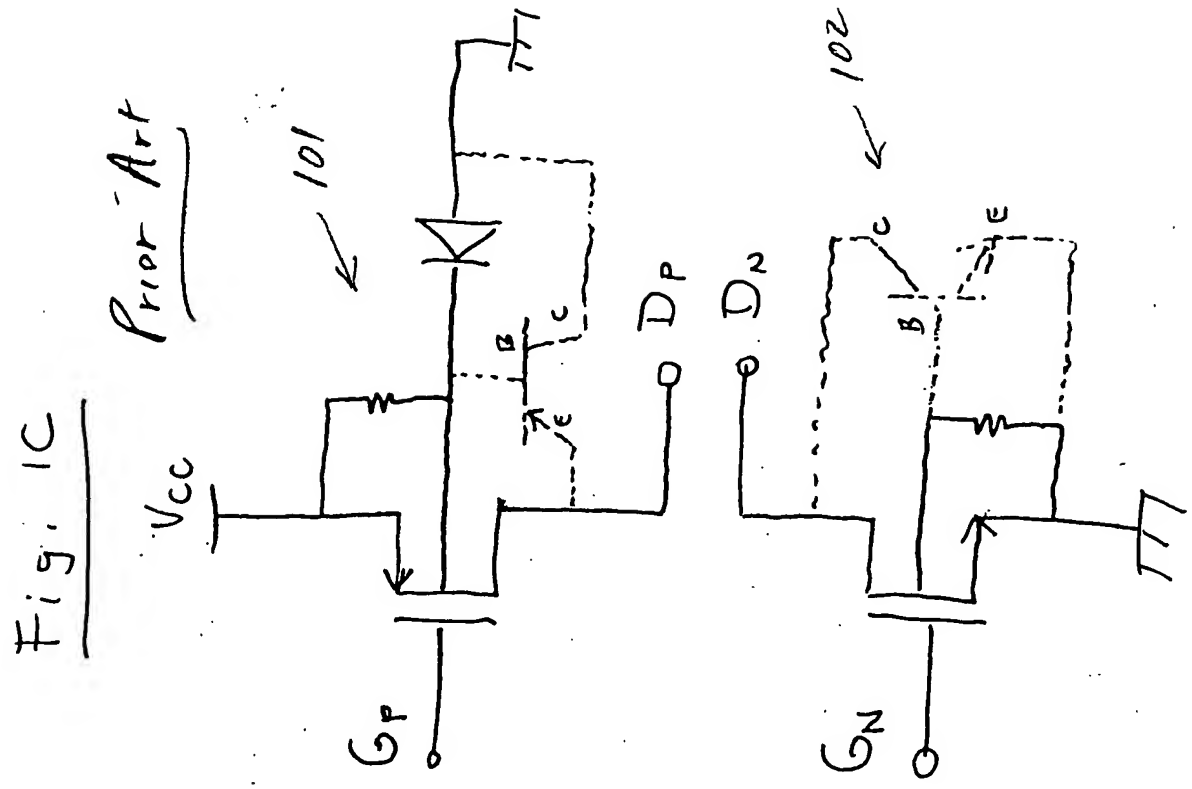
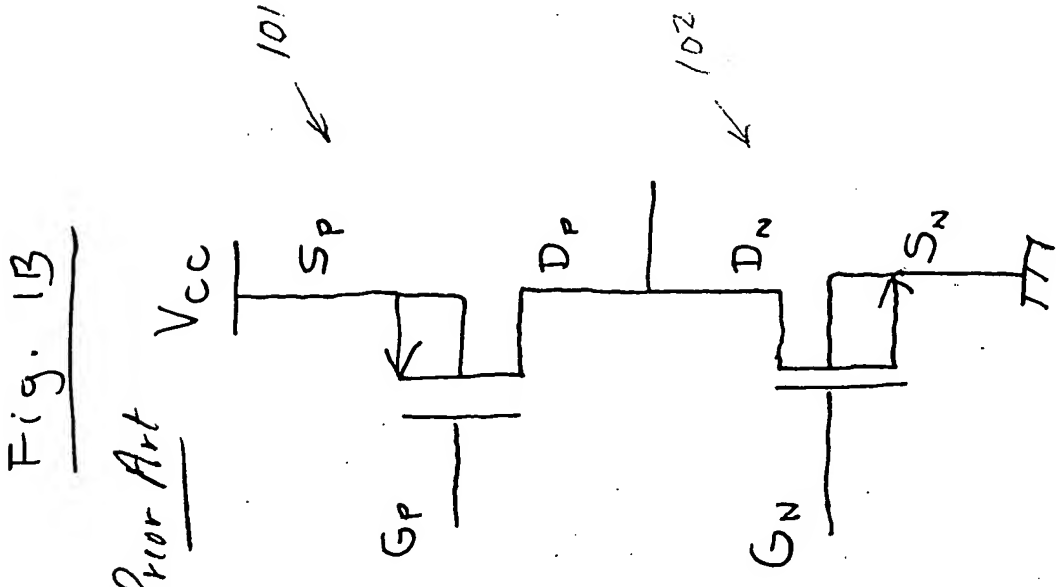
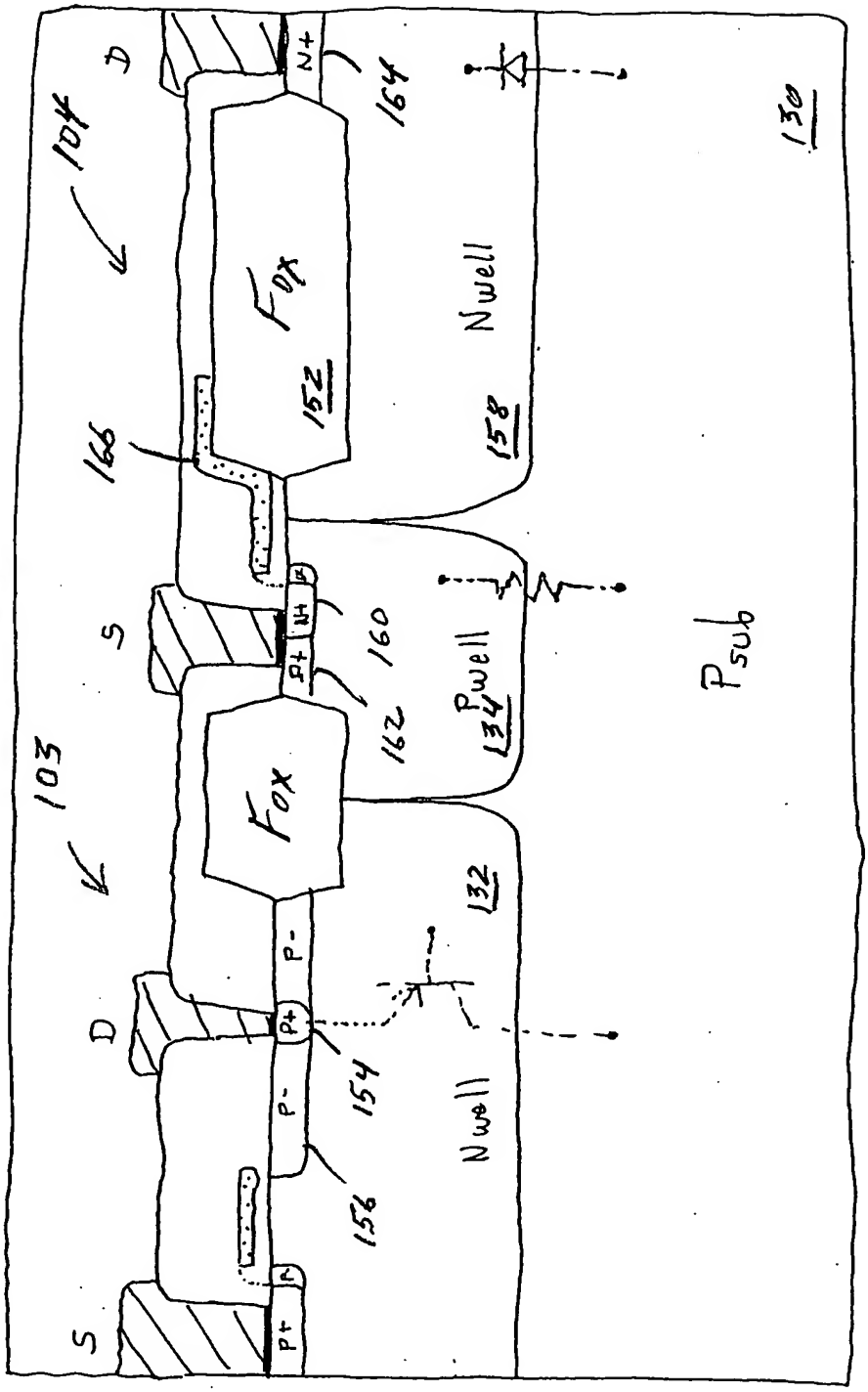


Fig. 1B
Prior Art





Prior Art

Fig. 2A

Fig. 2B

Prior Art

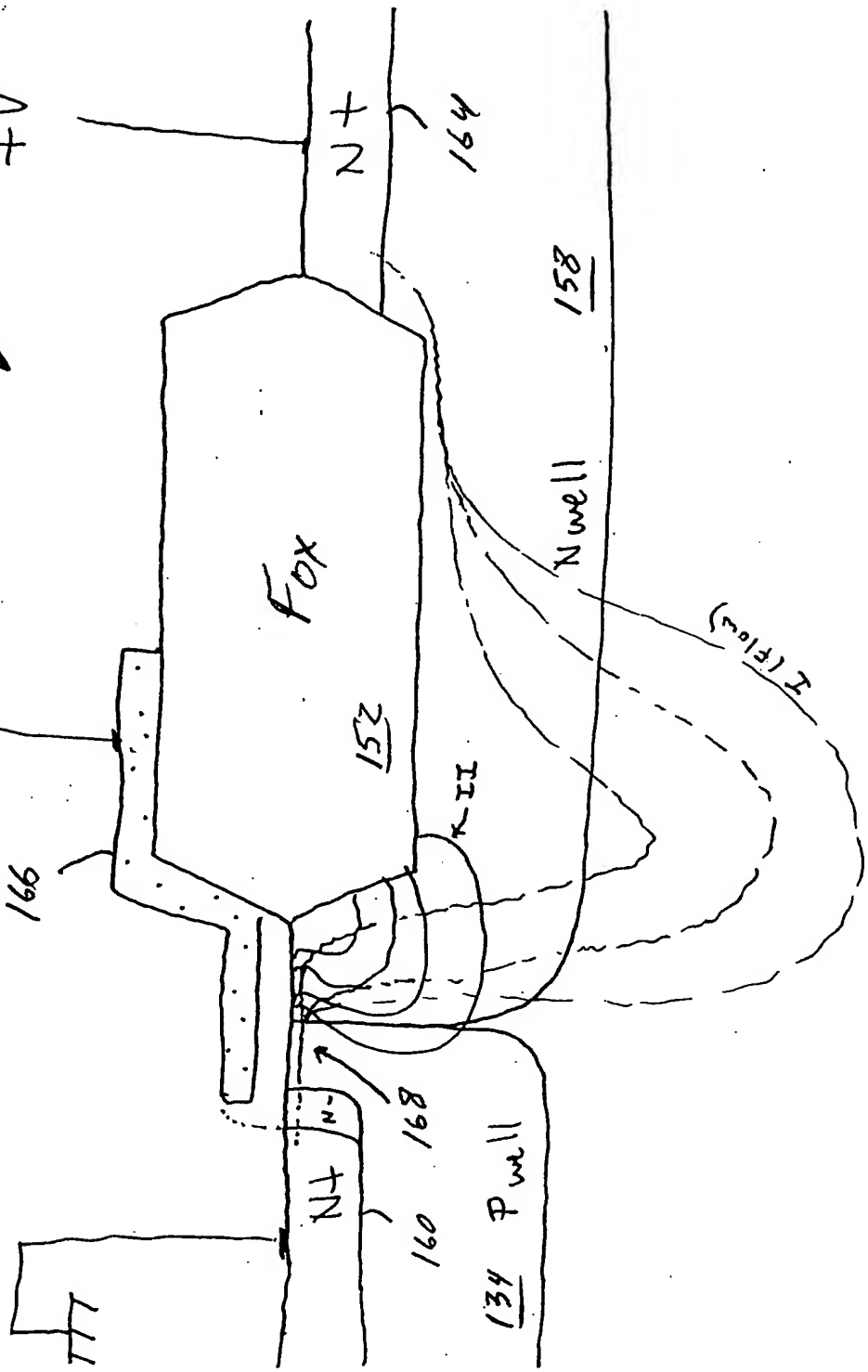
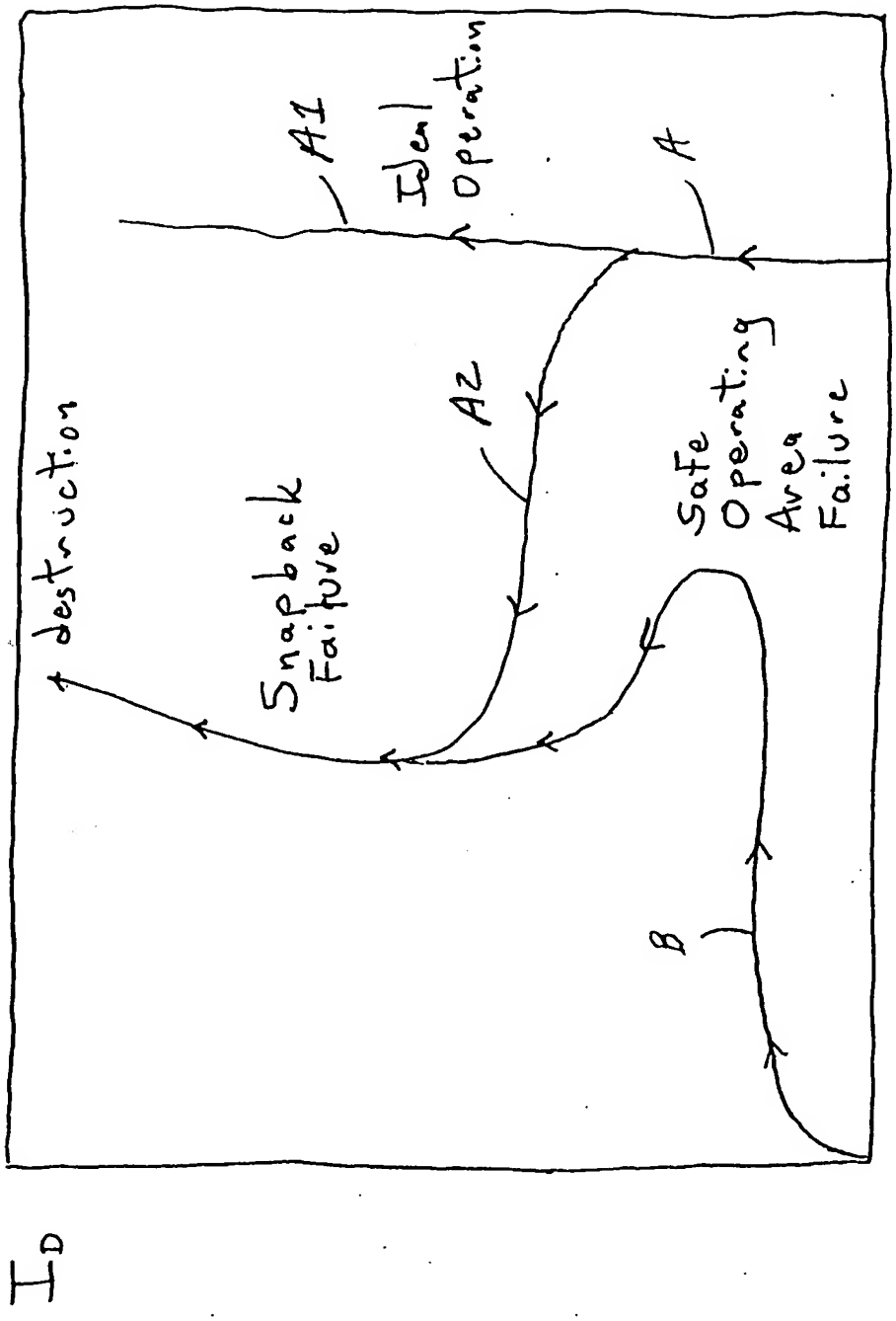
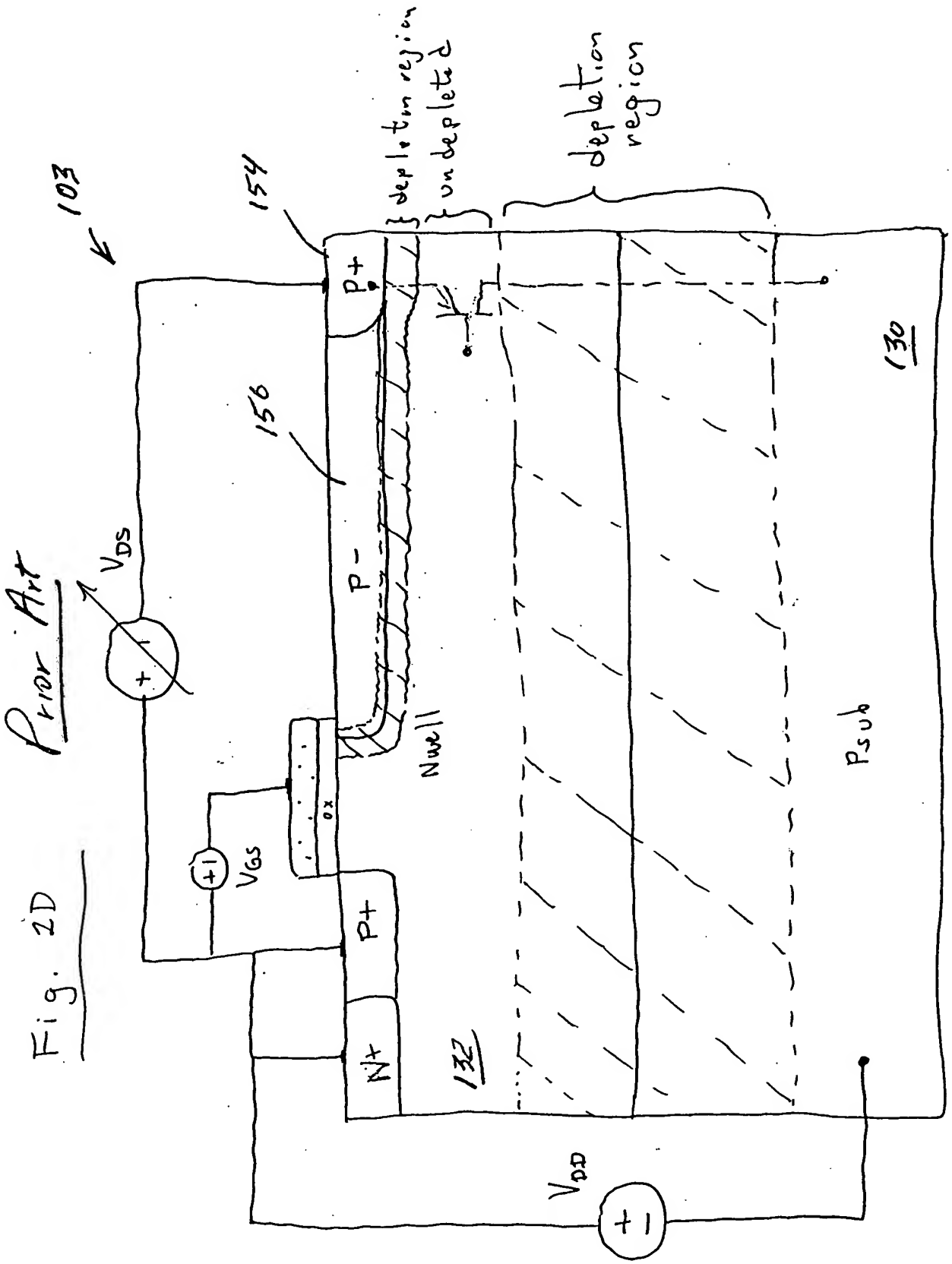


Fig 2C

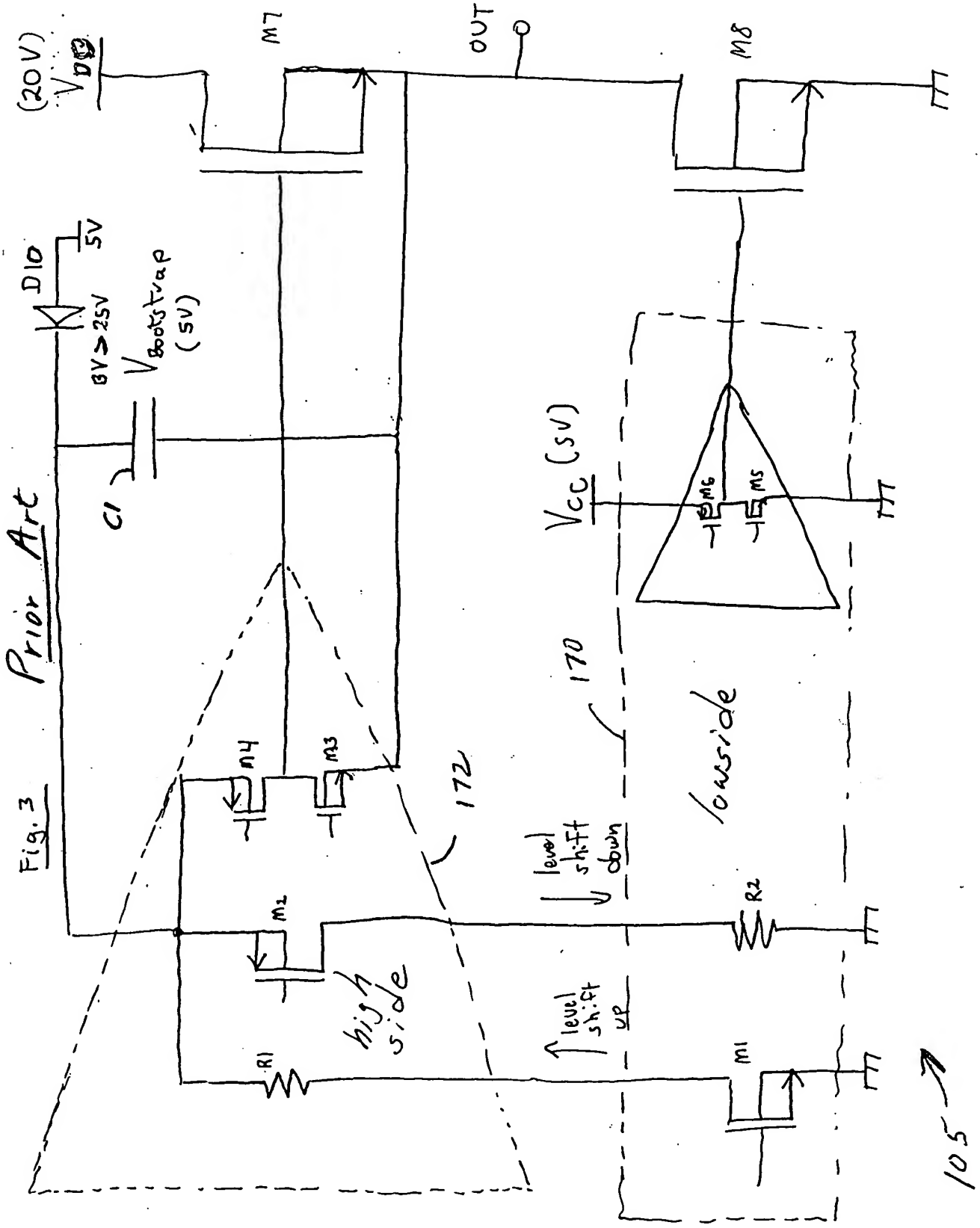
Prior Art





Prior Art

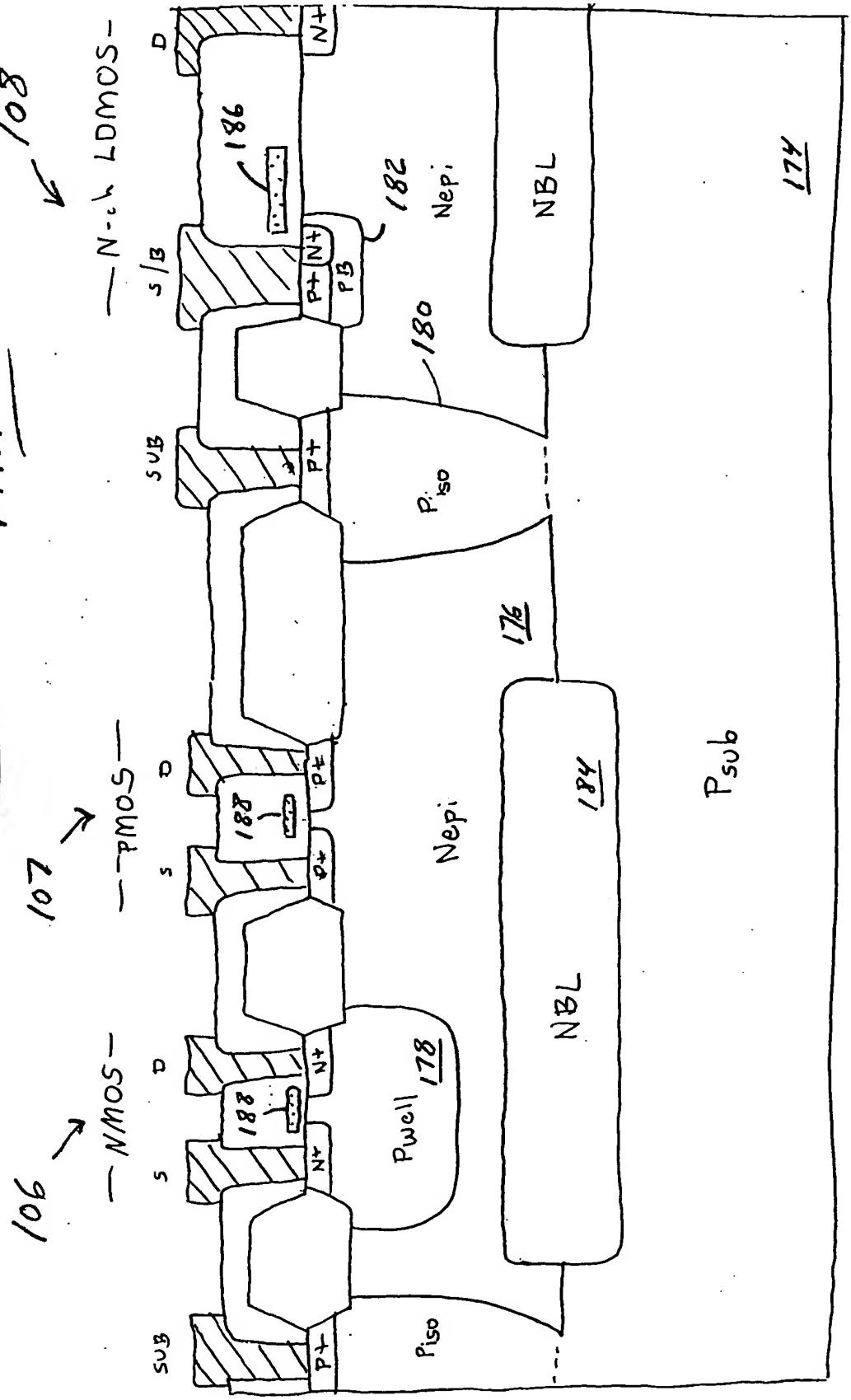
Fig. 2D



Prior Art

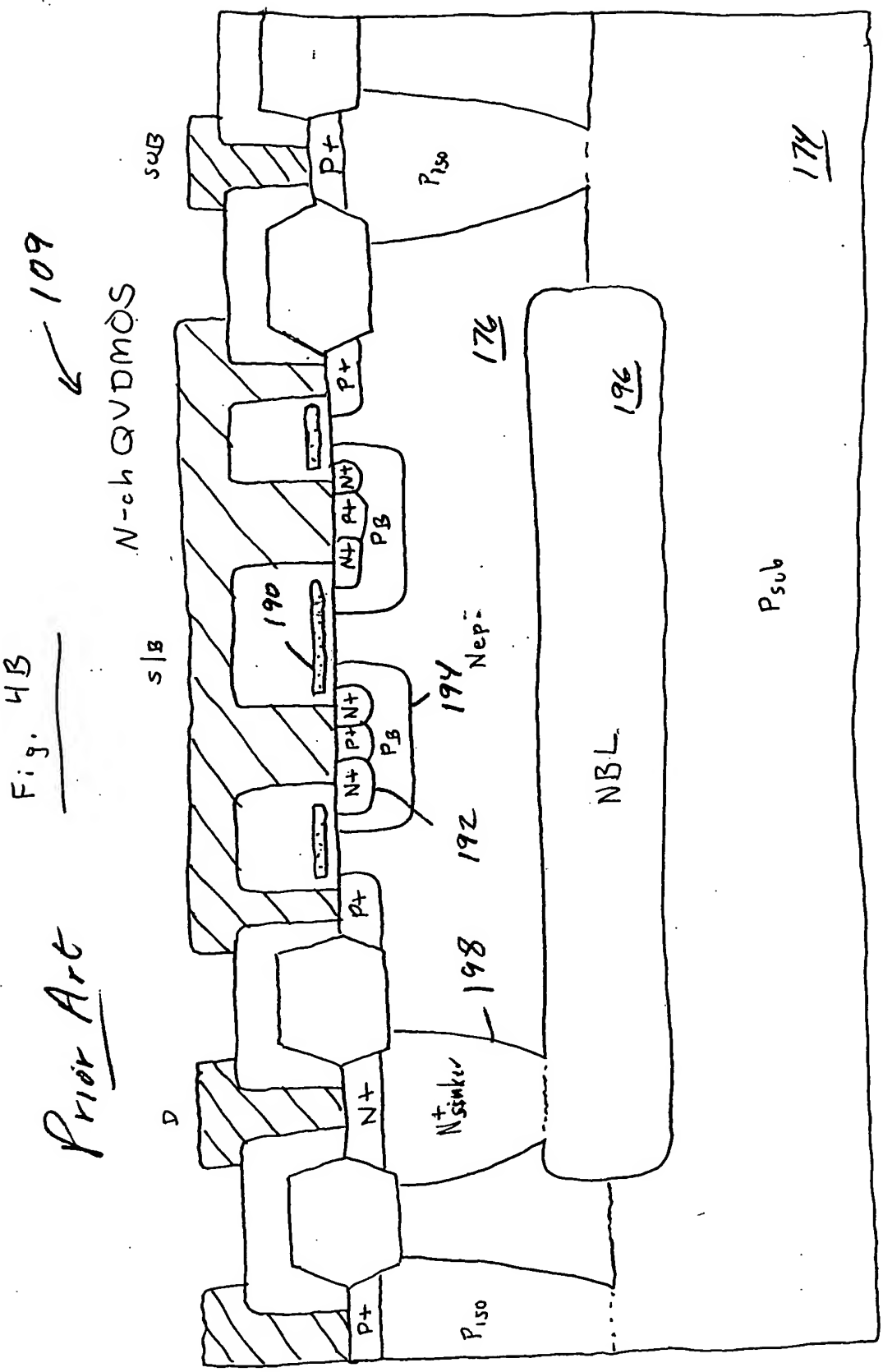
Fig. 3

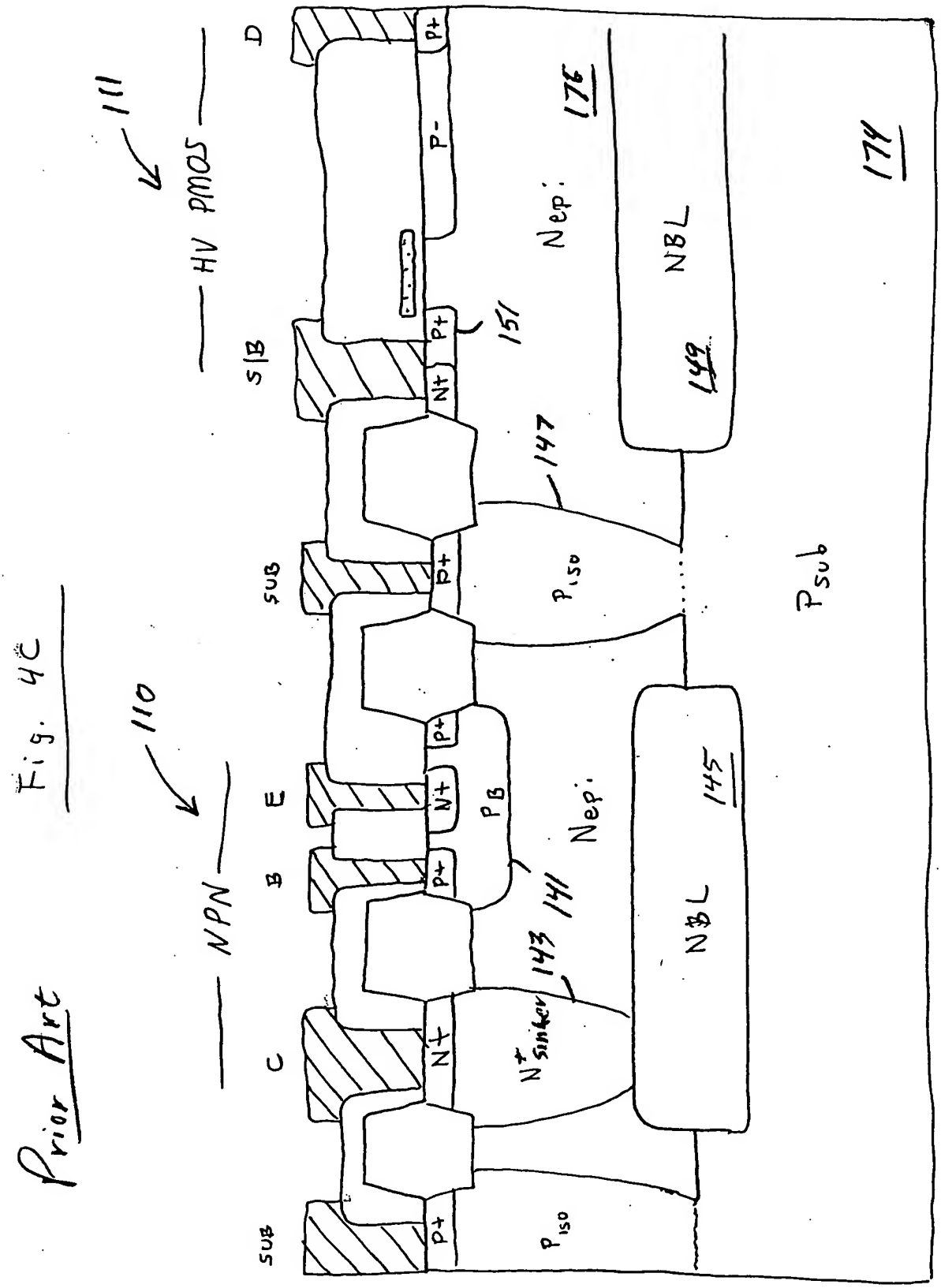
Fig. 4A Prior Art



Prior Art

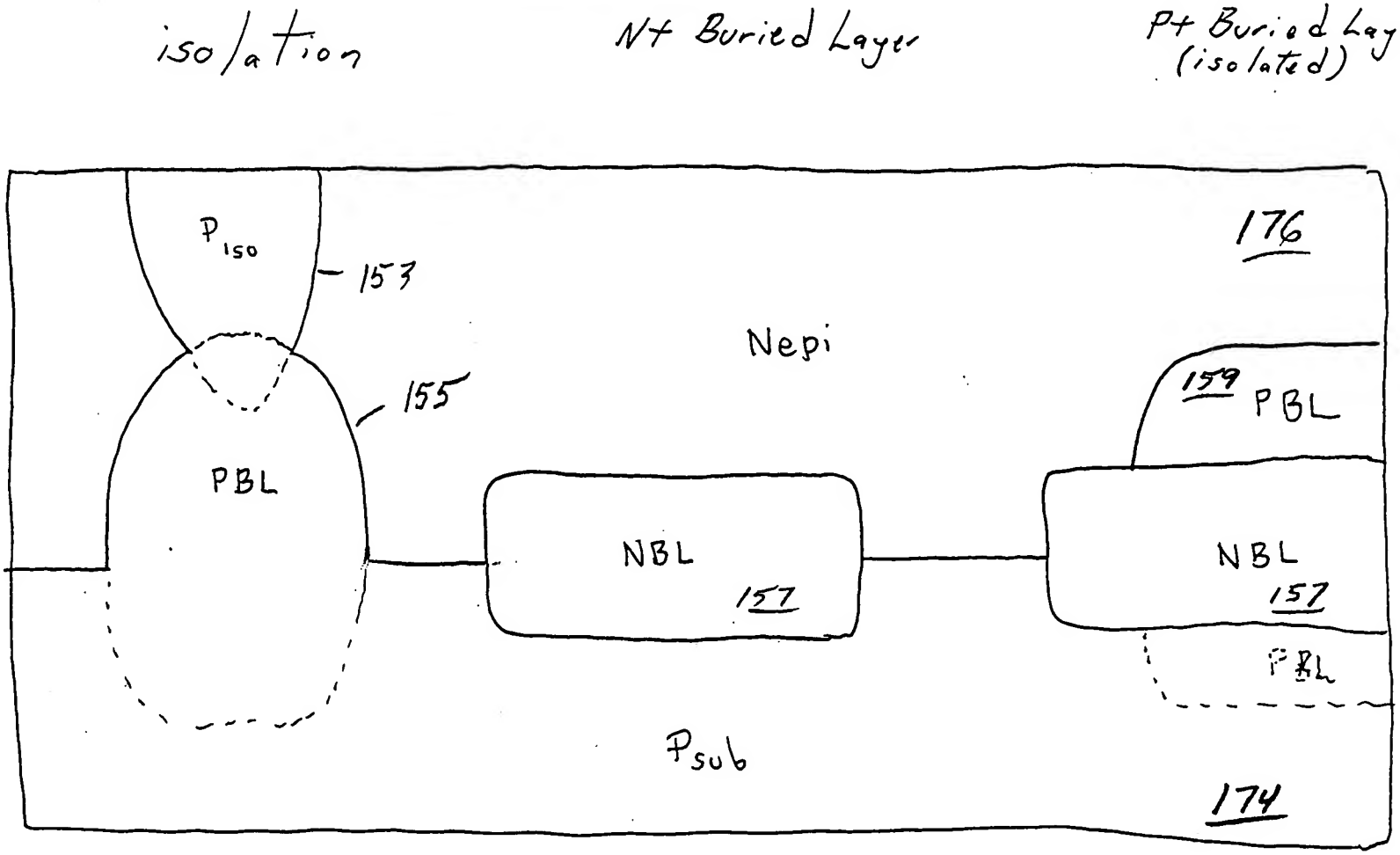
Fig. 4B




Prior Art
Fig. 4C
110
NPN
111
HV PMOS
C
B
E
SUB
SUB
S|B
D
P+
N+
P+
P+
N+
P+
P+
P-
P+
N+ sinker
143
141
PB
Nepi
151
147
Piso
Piso
Nepi
178
NBL
149
NBL
145
Psub
174

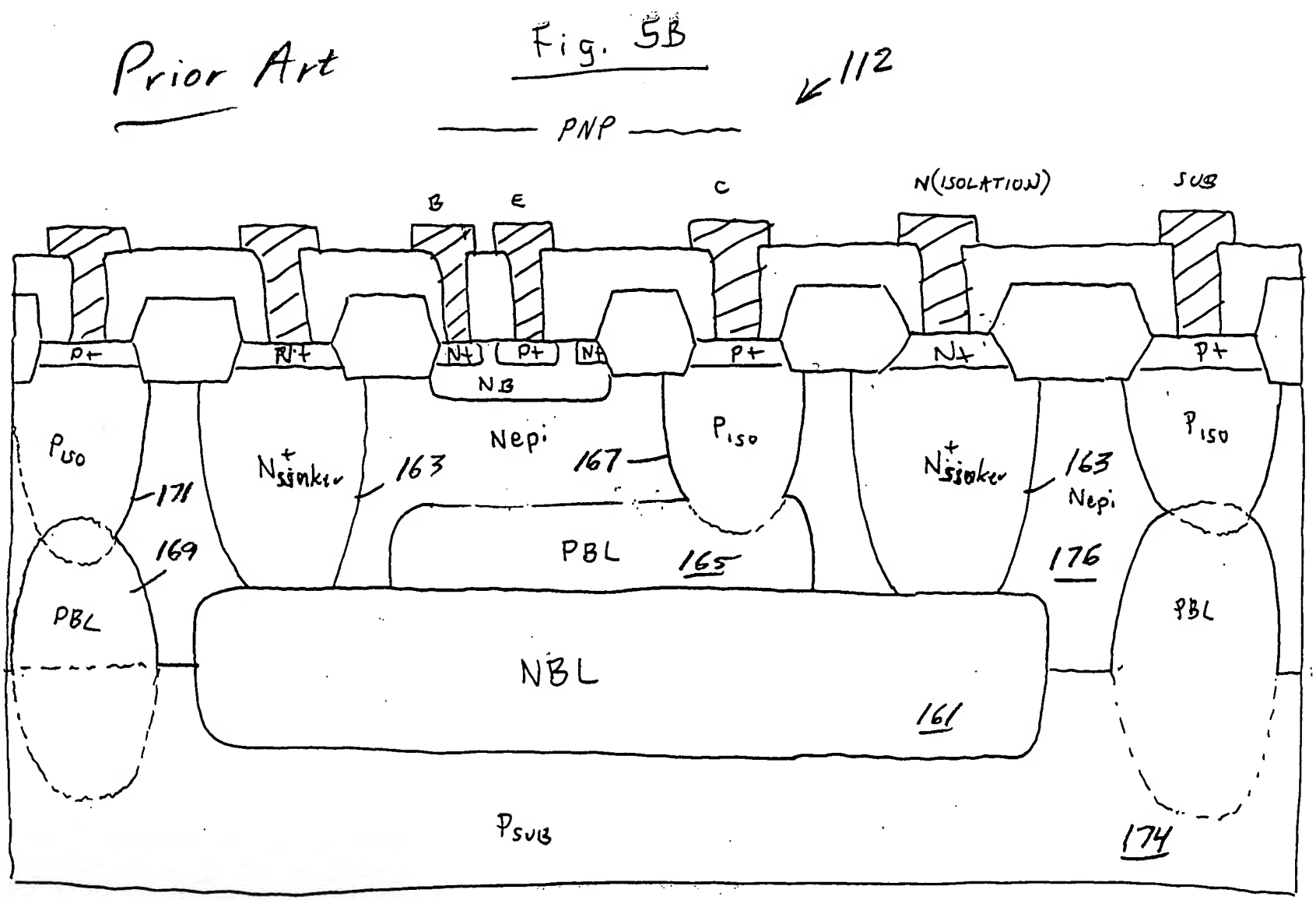
Prior Art

Fig. 5A



Prior Art

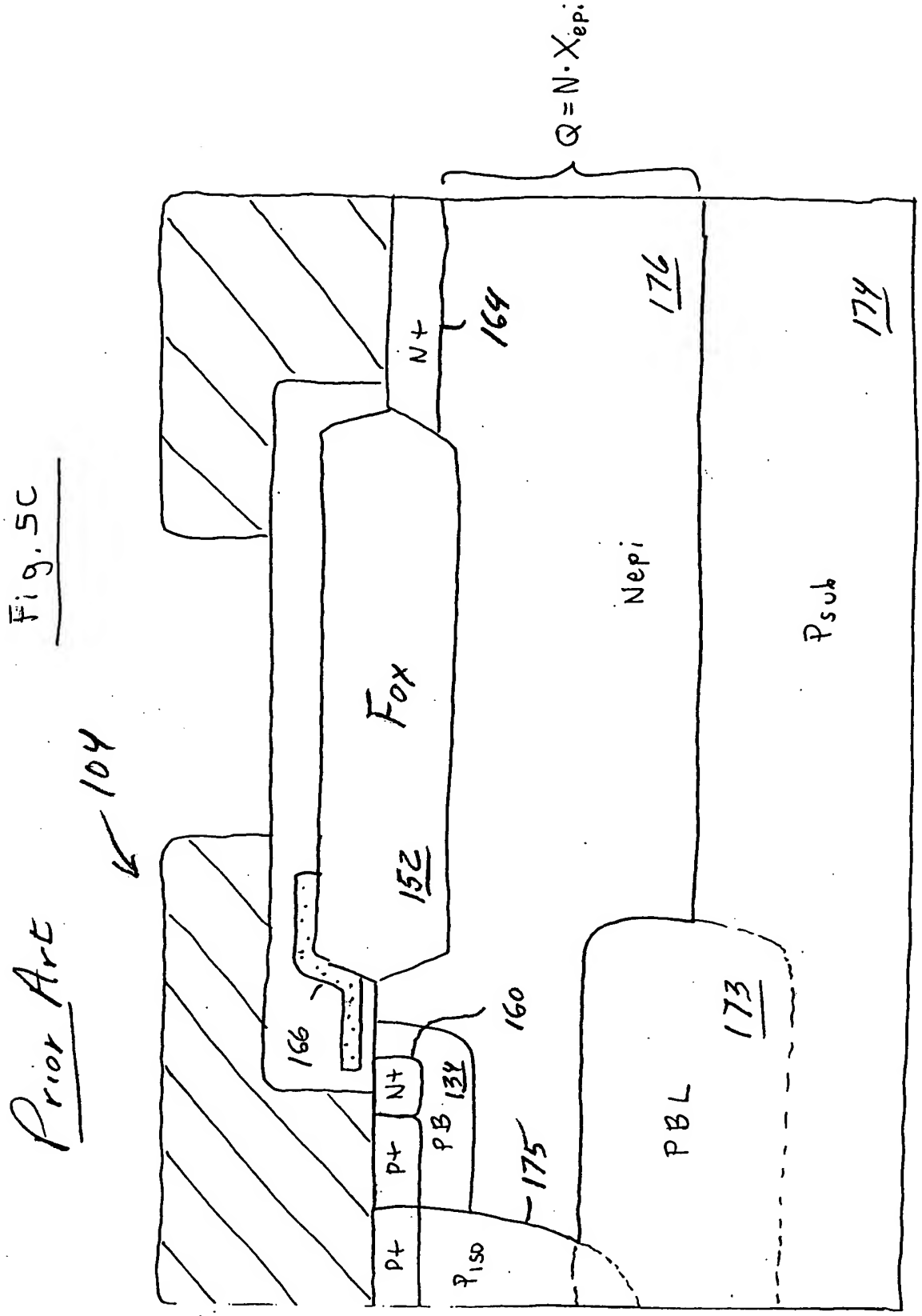
Fig. 5B



6/12/19

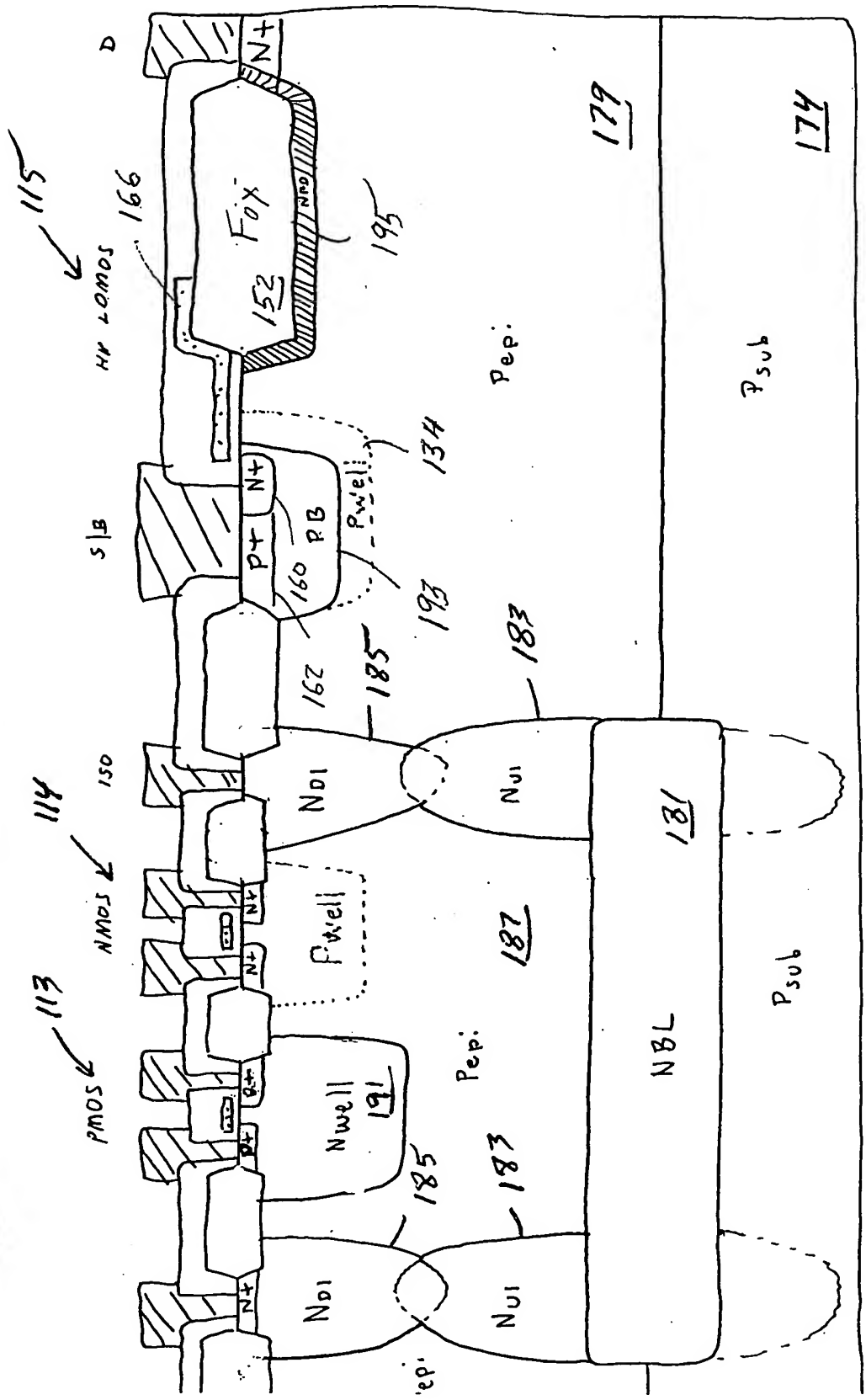
Fig. 5C

Prior Art



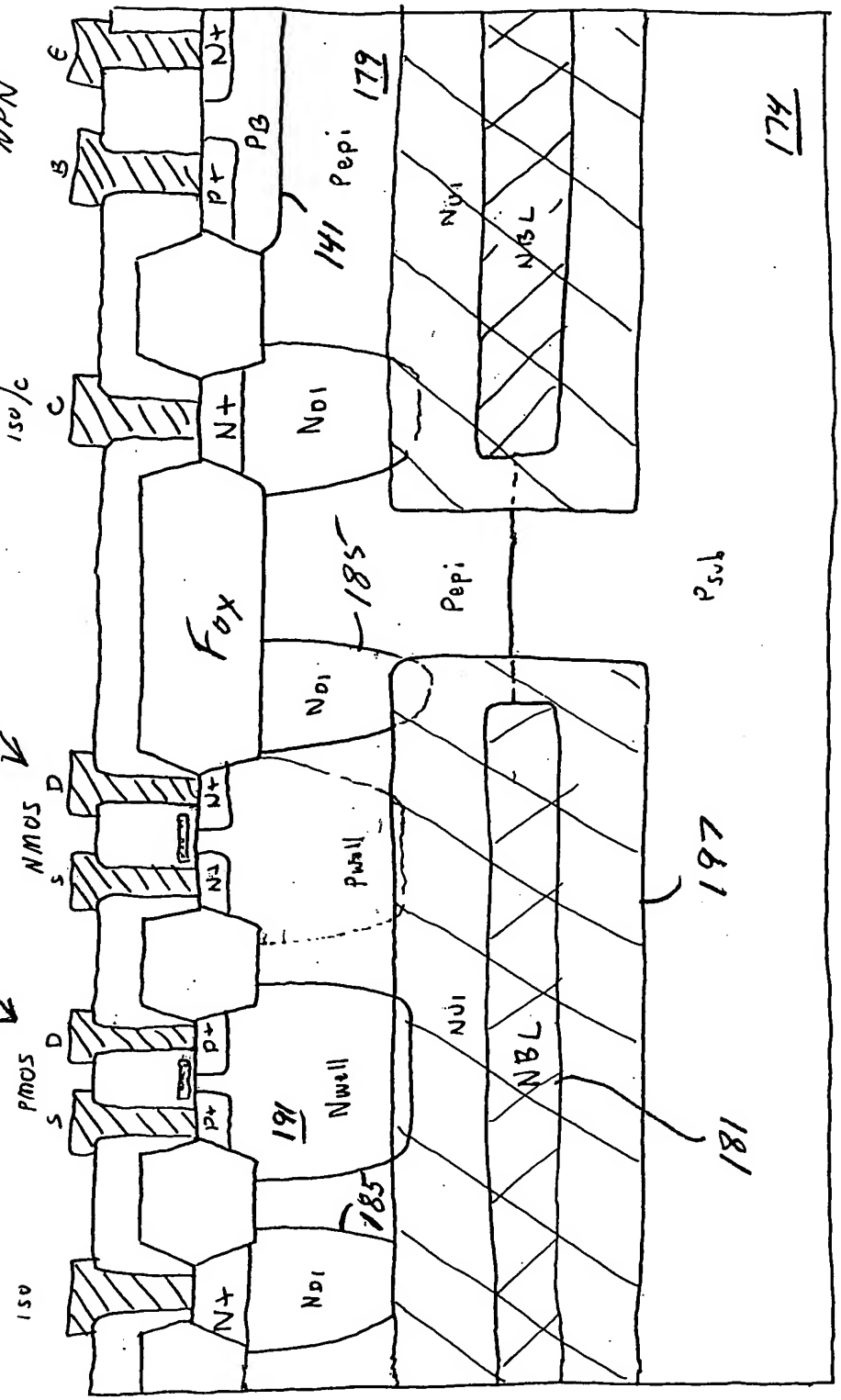
Prior Art

Fig 6A



Prior Art

Fig. 6B



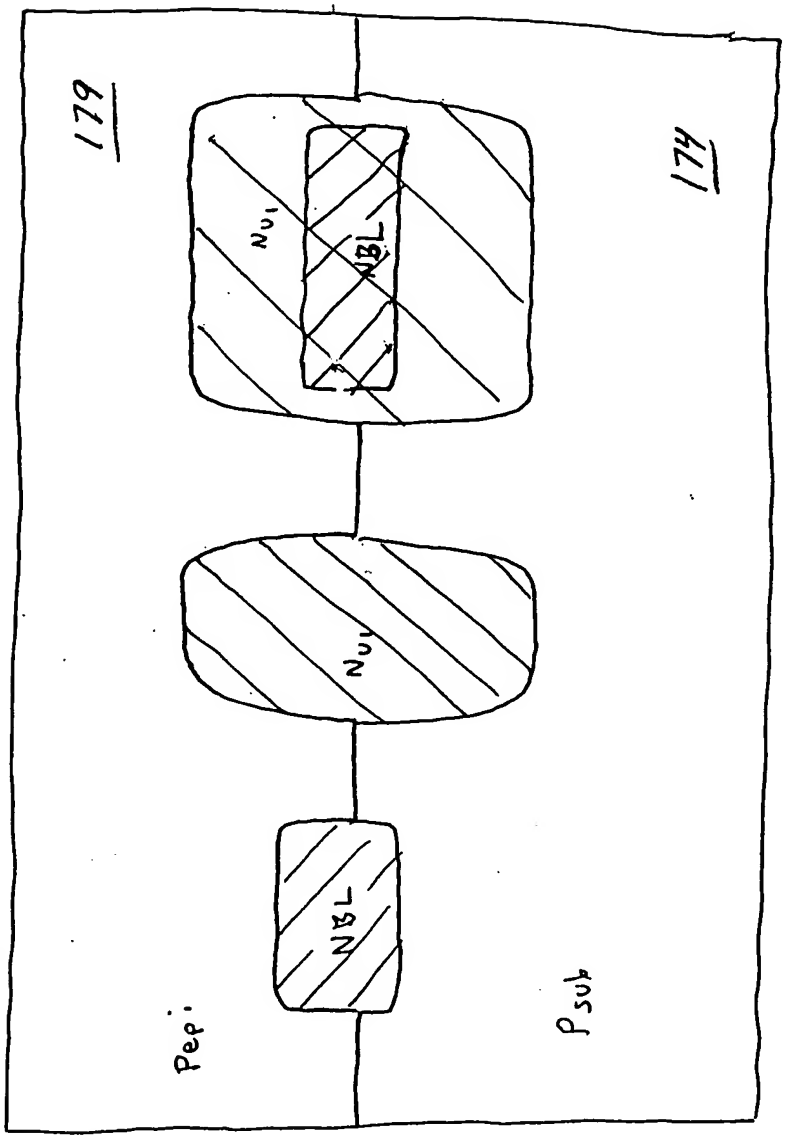


Fig. 6C

Prior Art

Prior Art

Fig. 7A

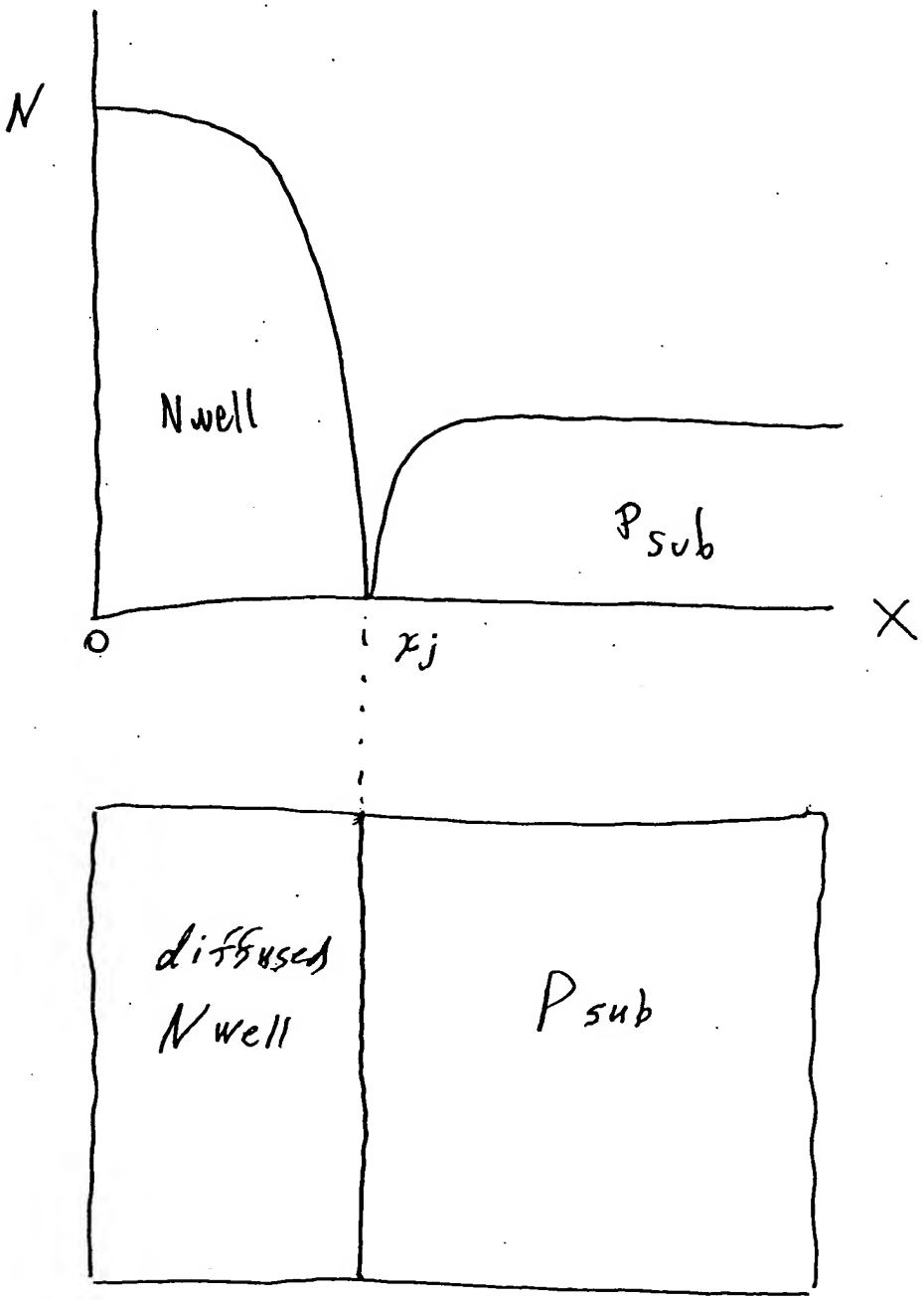


Fig. 7B

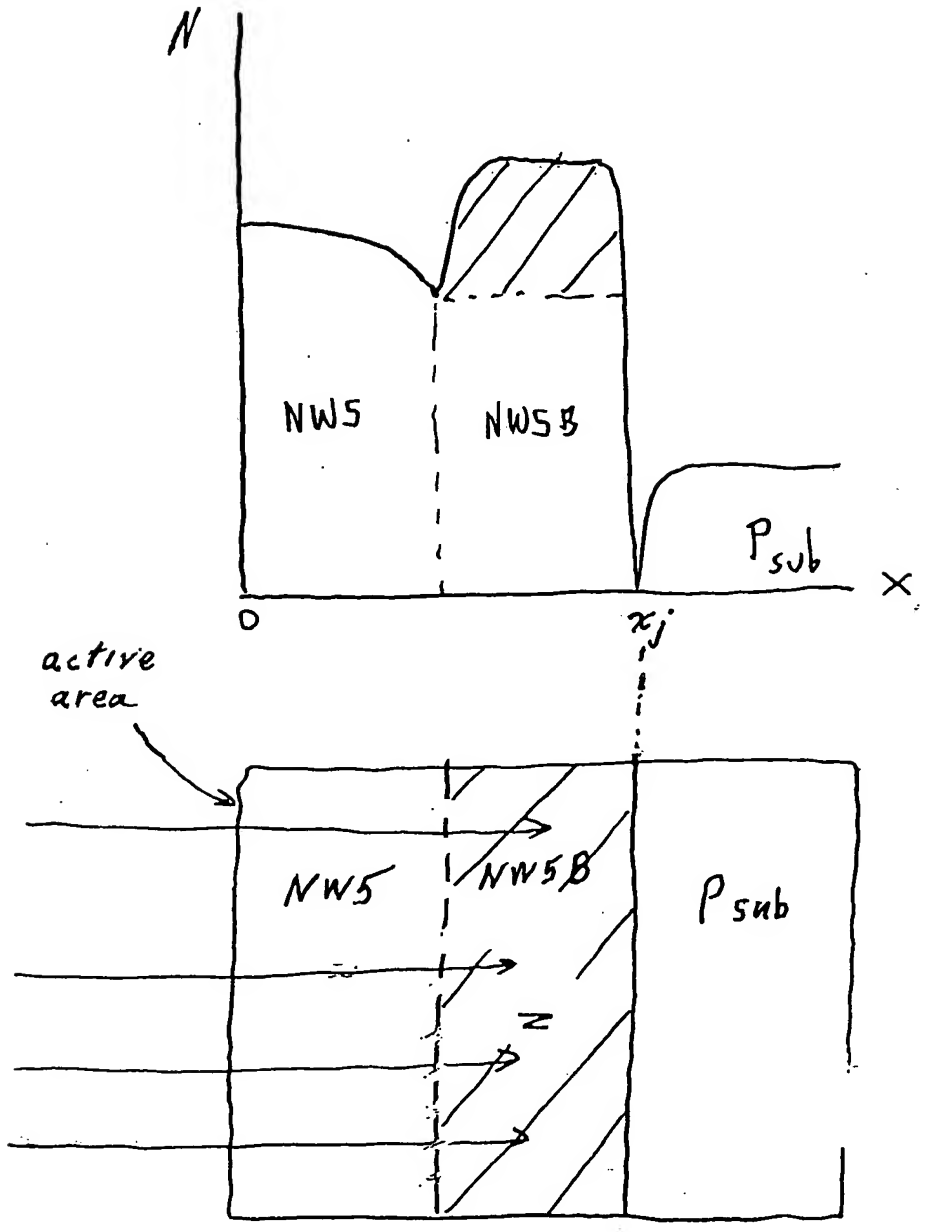


Fig. 7C

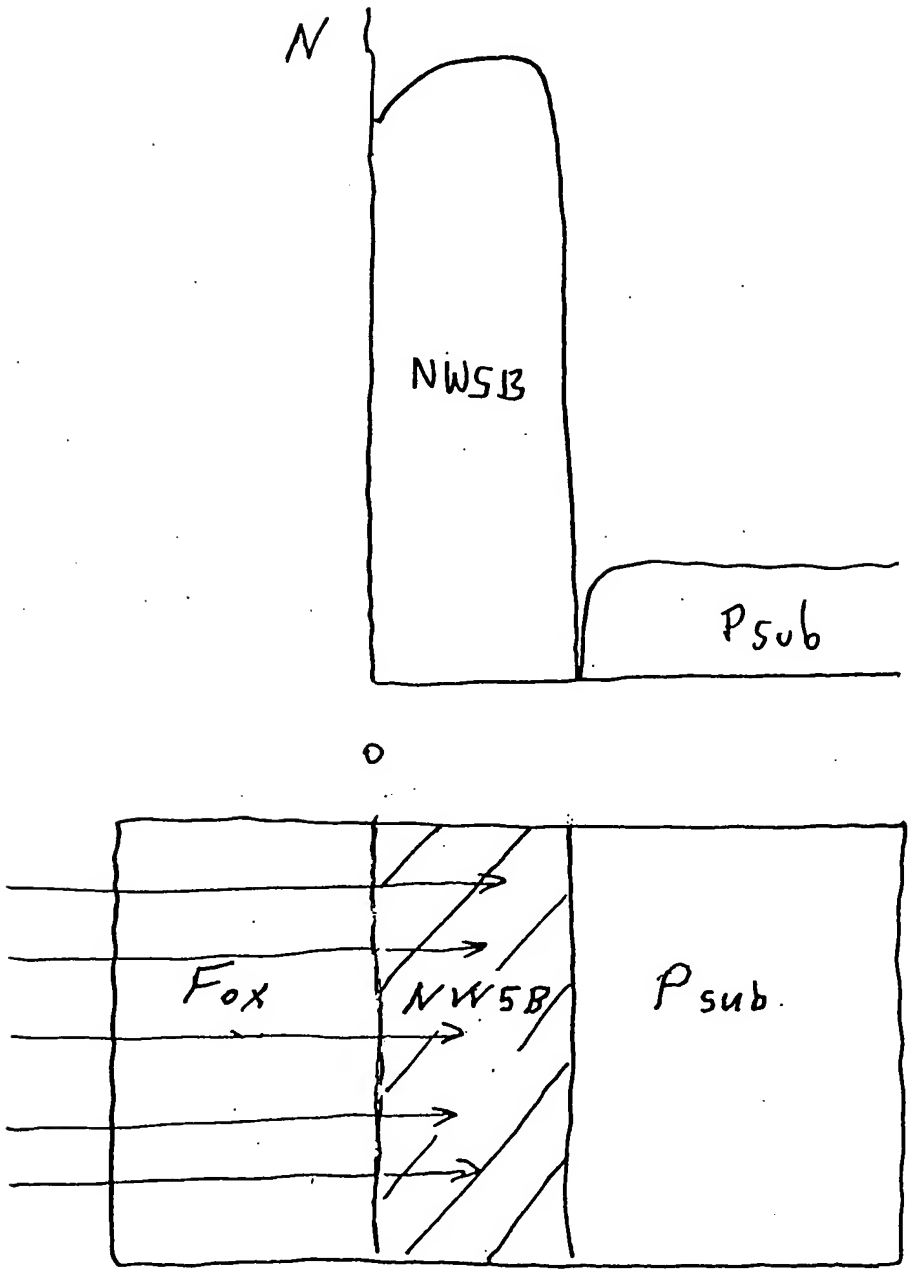


Fig. 8A

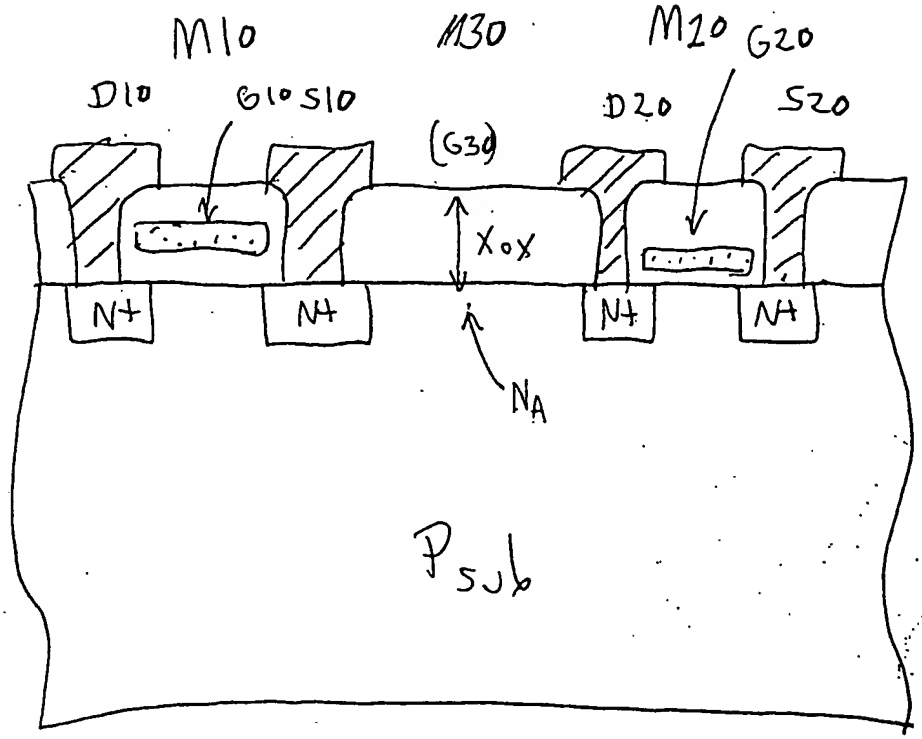
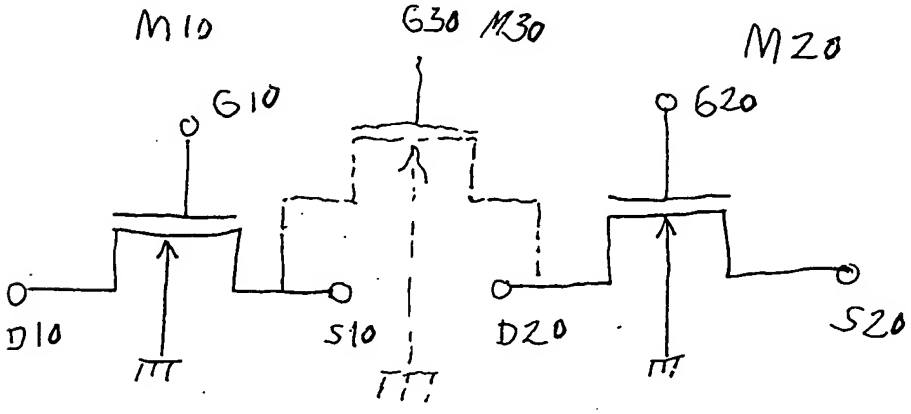

M10
M30
M20
G20
D10
G10
S10
D20
S20
(G30)
X_{OX}
N+
N+
N+
N+
N_A
P_{SUB}

Fig. 8B


M10
G30
M30
M20
G10
G20
D10
S10
D20
S20

Prior Art

Fig. 9A

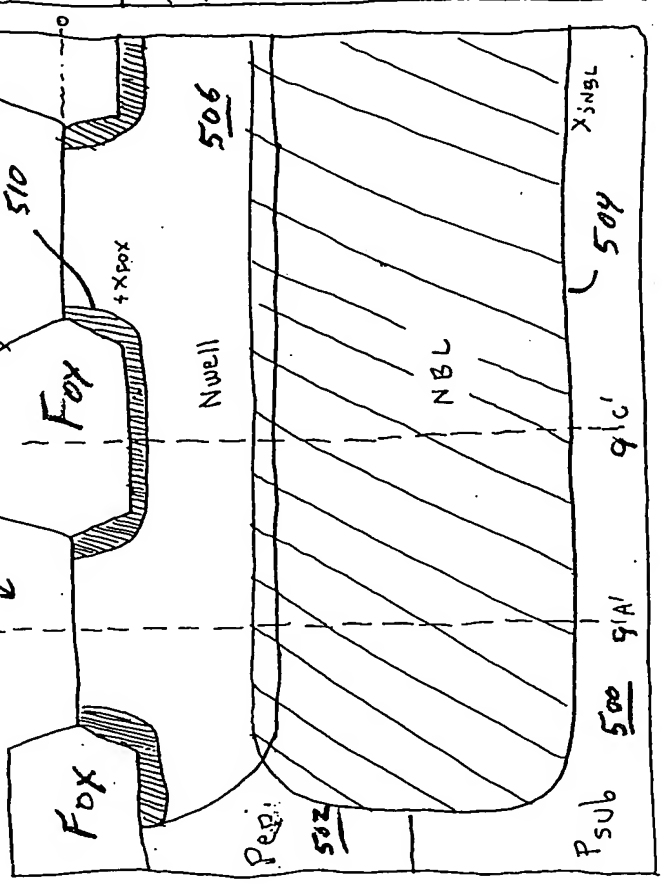
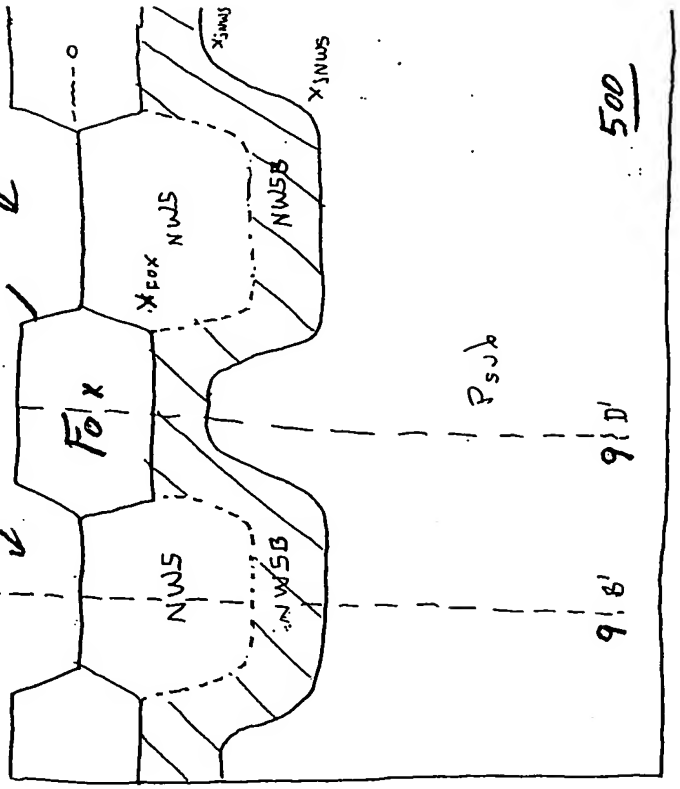


Fig. 9B



Prior Art

Fig. 9C

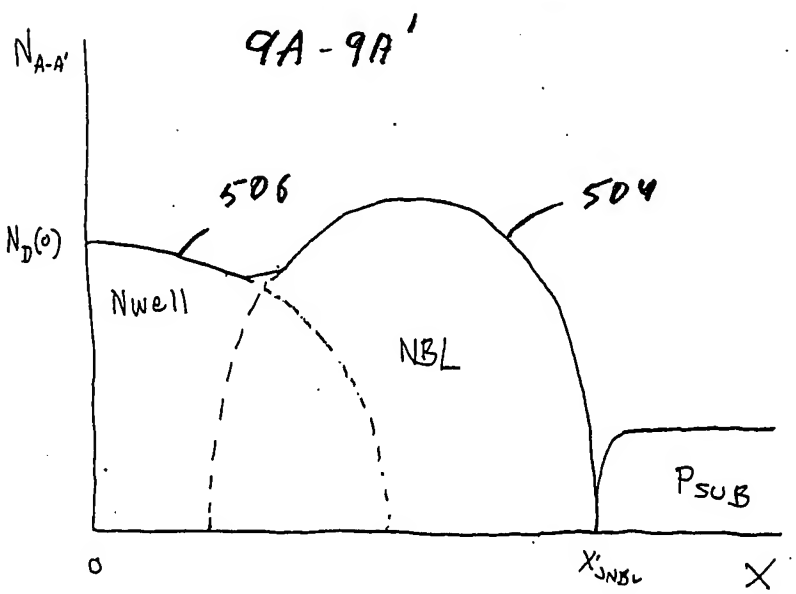
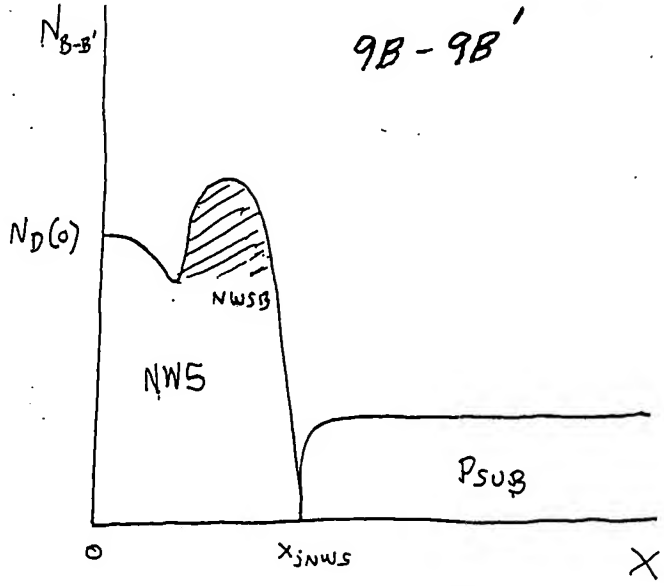


Fig. 9D



Prior Art

Fig. 9E

9C-9C'

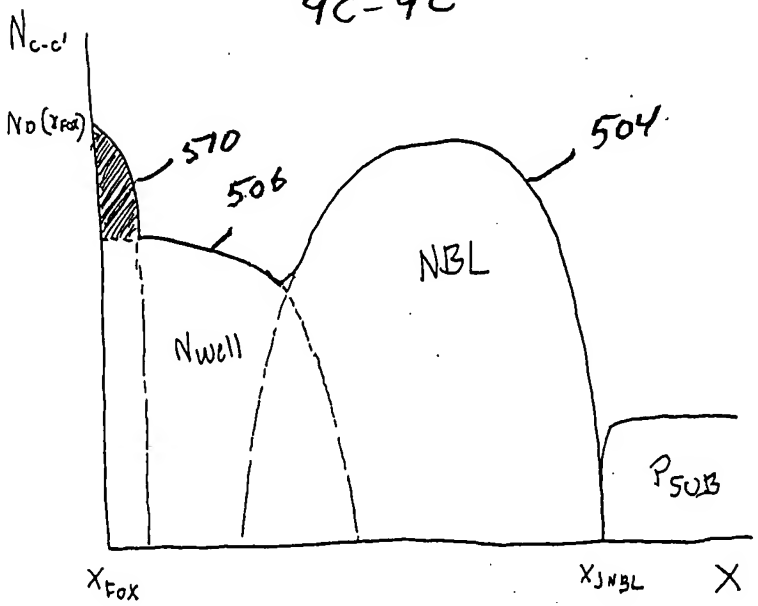
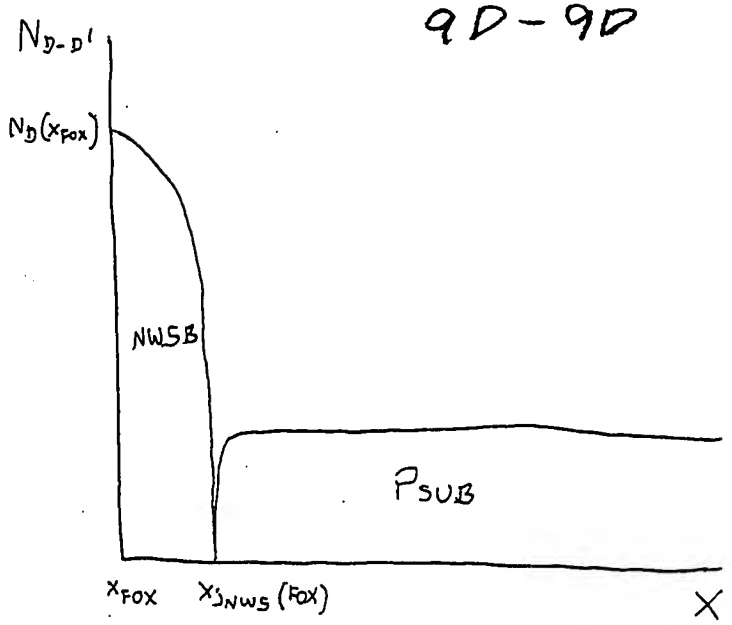


Fig. 9F

9D-9D'



Prior Art

Fig. 10A

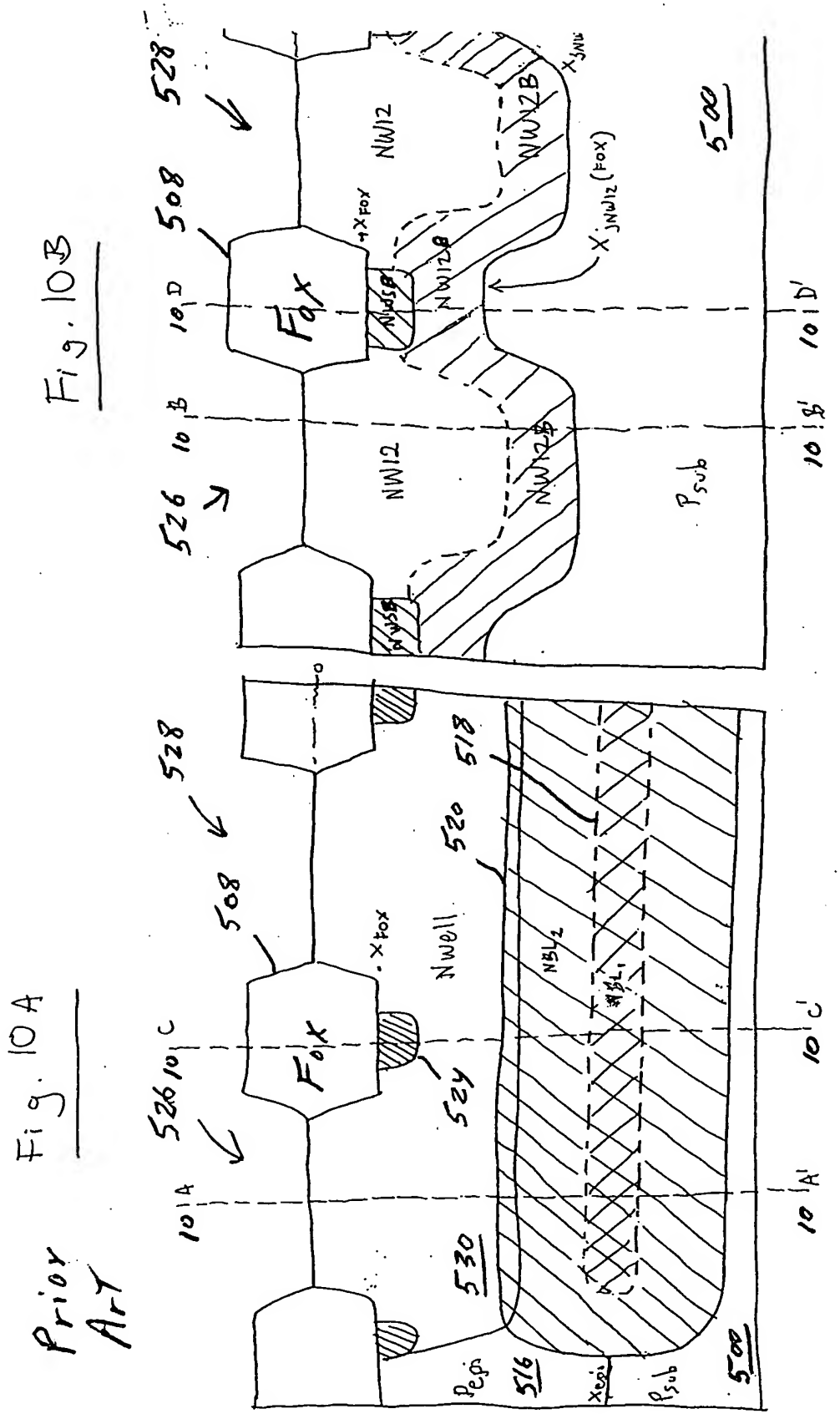


Fig. 10B

Fig. 10C

Prior Art

10A - 10A'

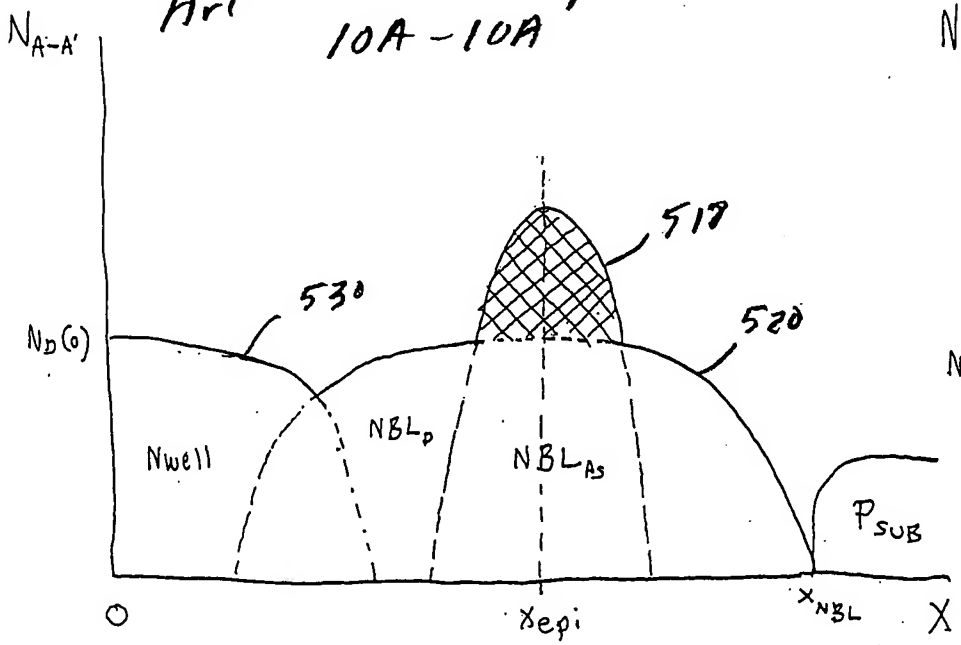


Fig. 10D

10B - 10B'

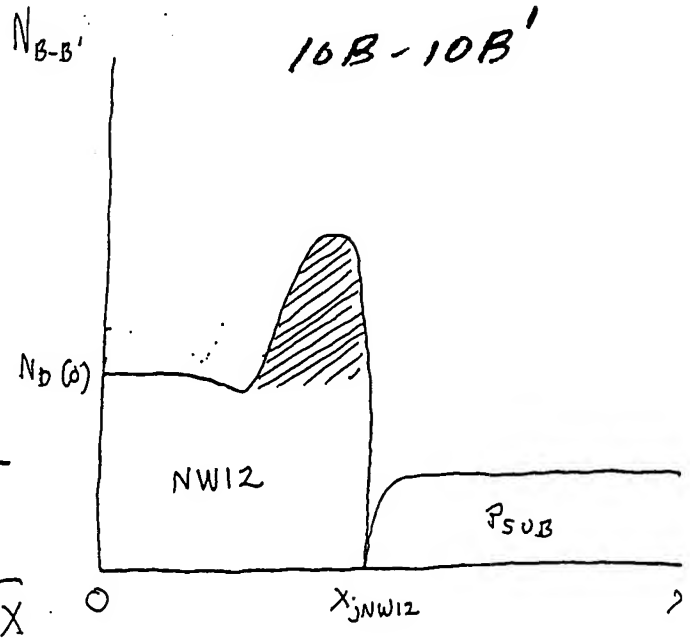
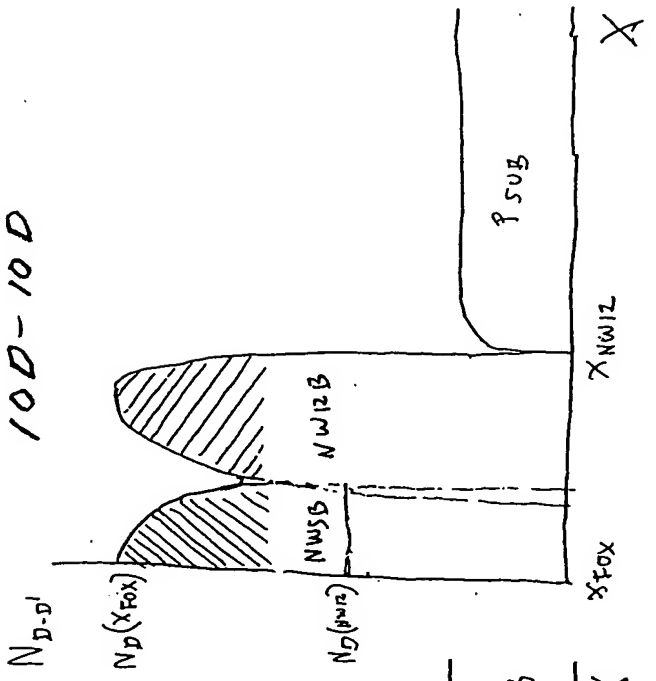


Fig. 10F

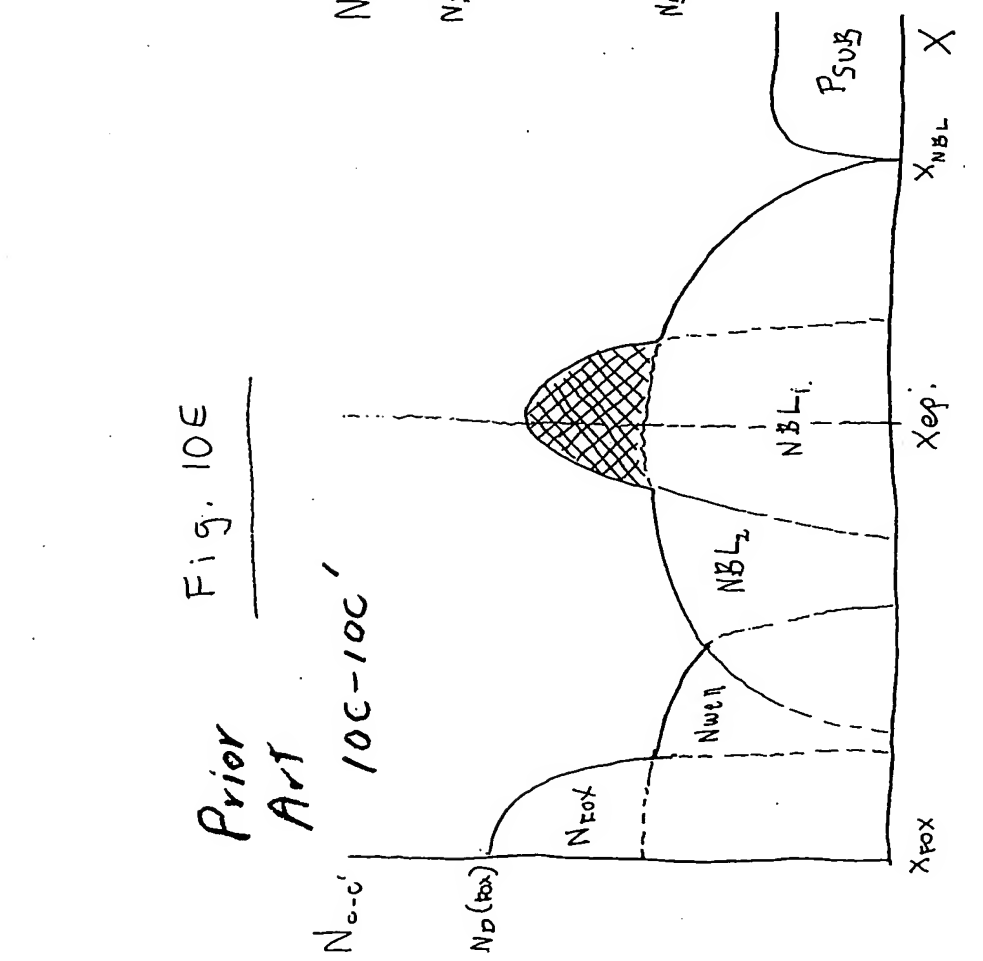
10D-10D'



Prior Art

Fig. 10E

10C-10C'



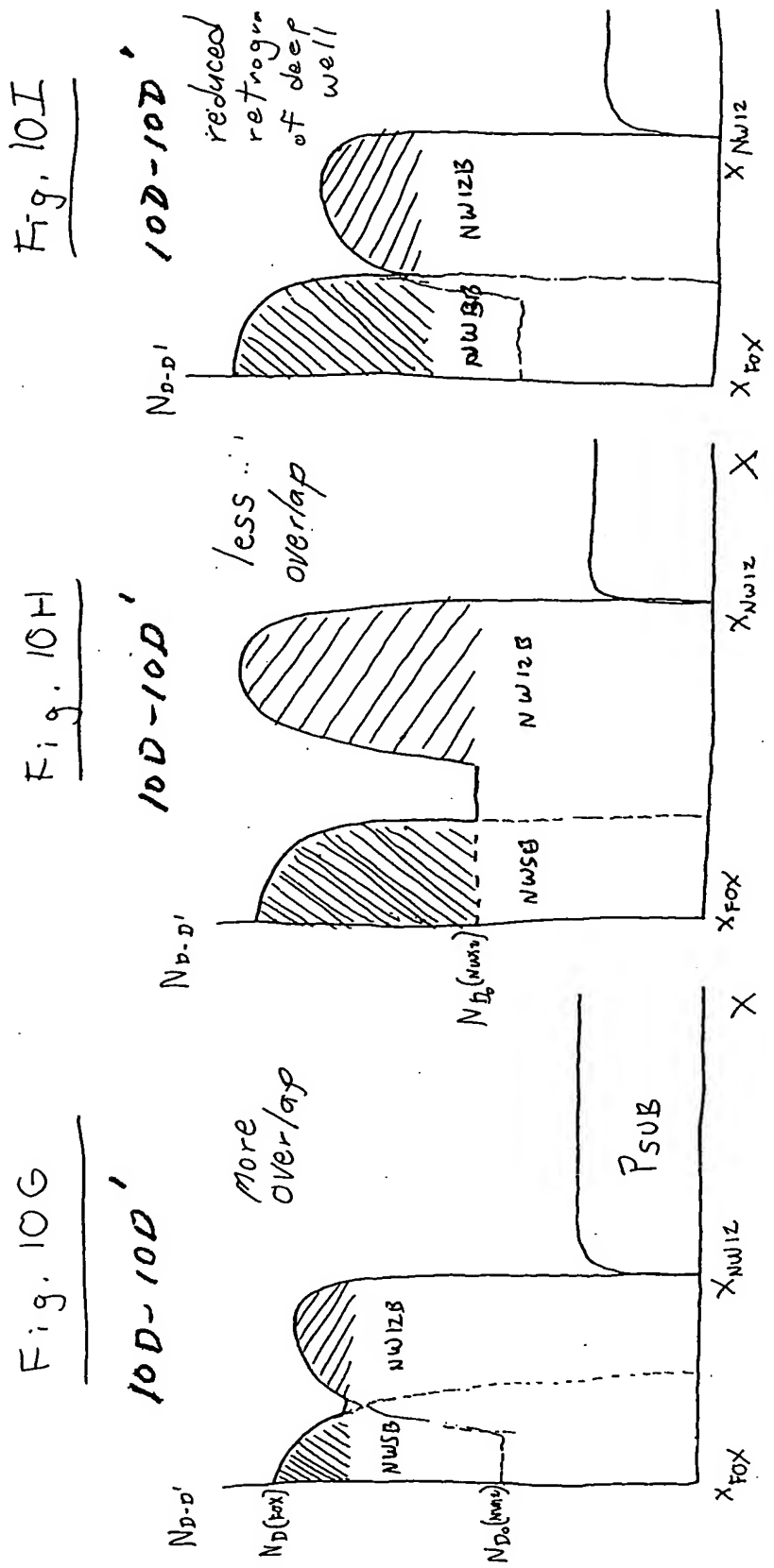


Fig. 10G
10D-10D'
More overlap
$N_{D-D'}$
$N_{D(FOX)}$
$N_{D(NW12)}$
NWSB
NW12B
PSUB
X_{NW12}
X_{FOX}
Fig. 10H
10D-10D'
less overlap
$N_{D-D'}$
$N_{D(NW12)}$
NWSB
NW12B
X_{NW12}
X_{FOX}
Fig. 10I
10D-10D'
reduced retrogr. of deep well
$N_{D-D'}$
NWSB
NW12B
X_{NW12}
X_{FOX}

Fig. 10J

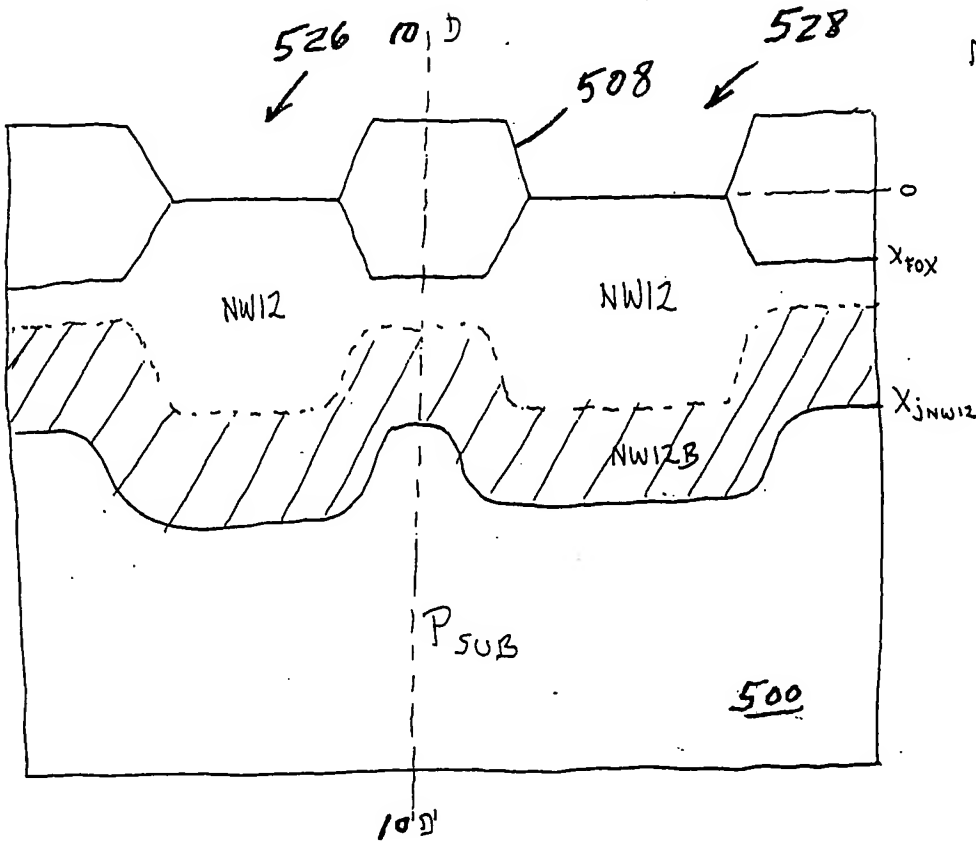
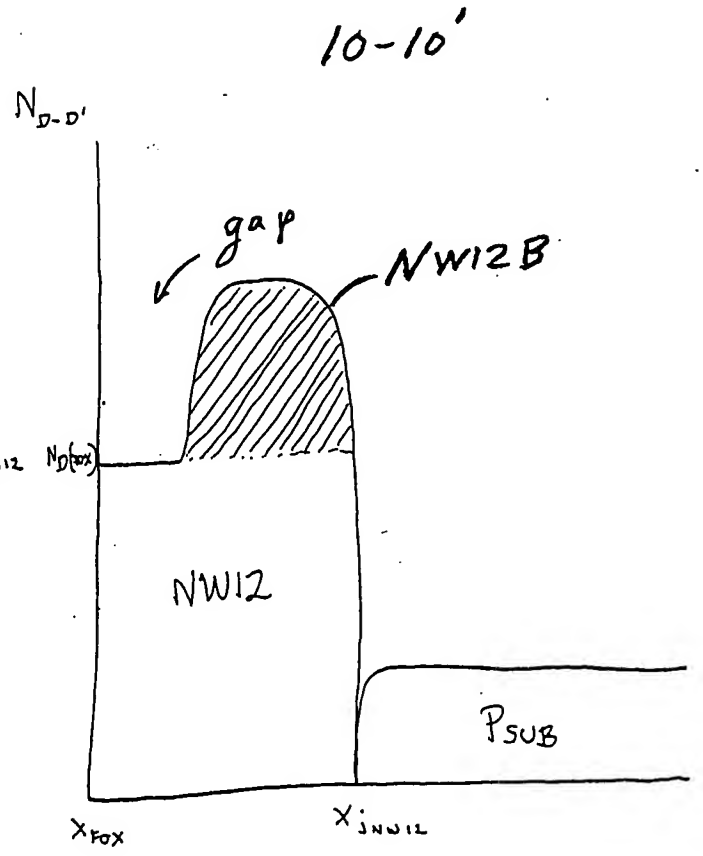


Fig. 10K



6/12/84

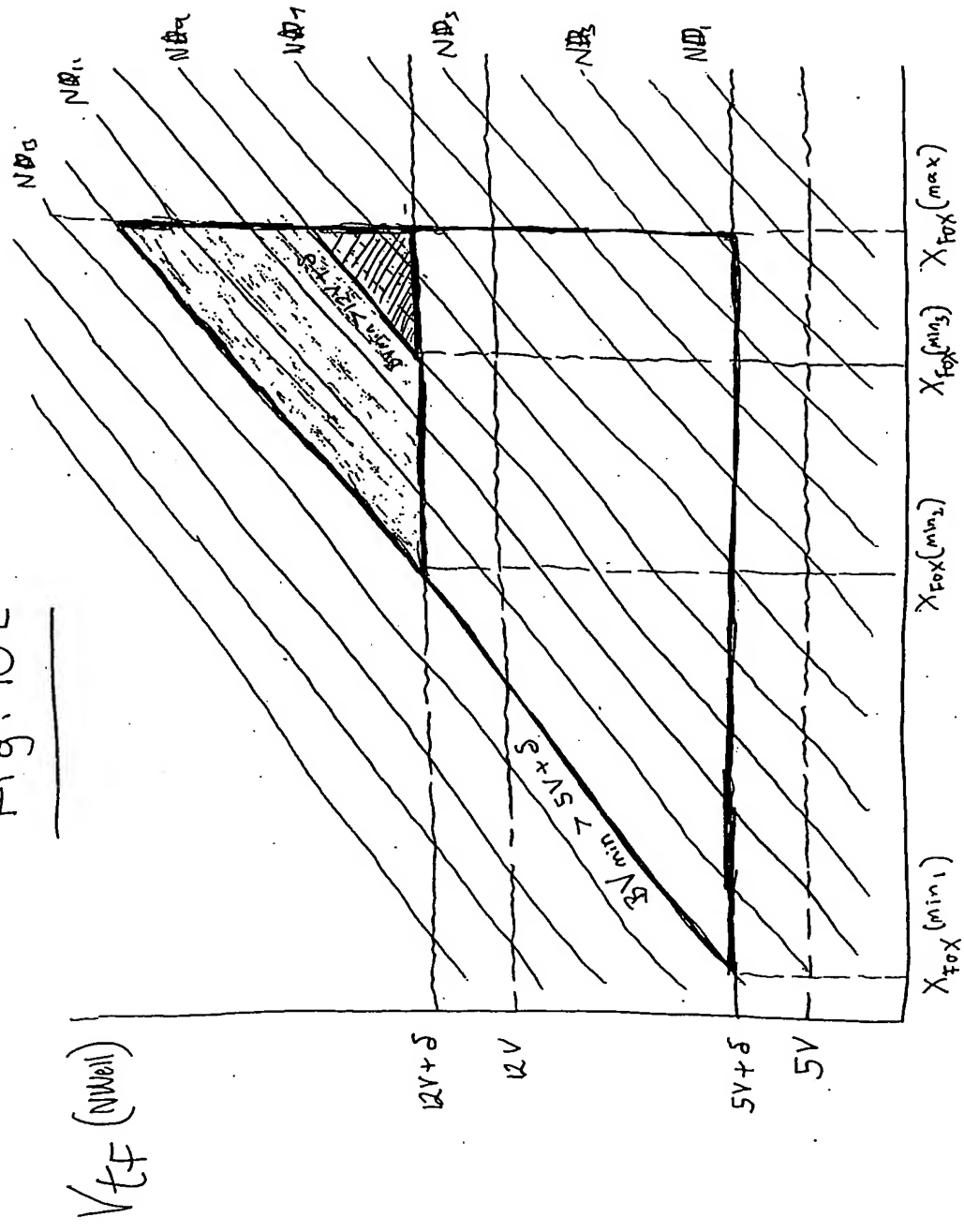

V_{tf} (NWell)
X_{FOX}
$X_{FOX(min_1)}$
$X_{FOX(min_2)}$
$X_{FOX(min_3)}$
$X_{FOX(max)}$
12V+δ
12V
5V+δ
5V
$BV_{min} > 5V_{x+δ}$
$BV_{min} > 12V_{x+δ}$
ND1
ND2
ND3
ND4
ND5
ND6
ND7

Fig. 10L

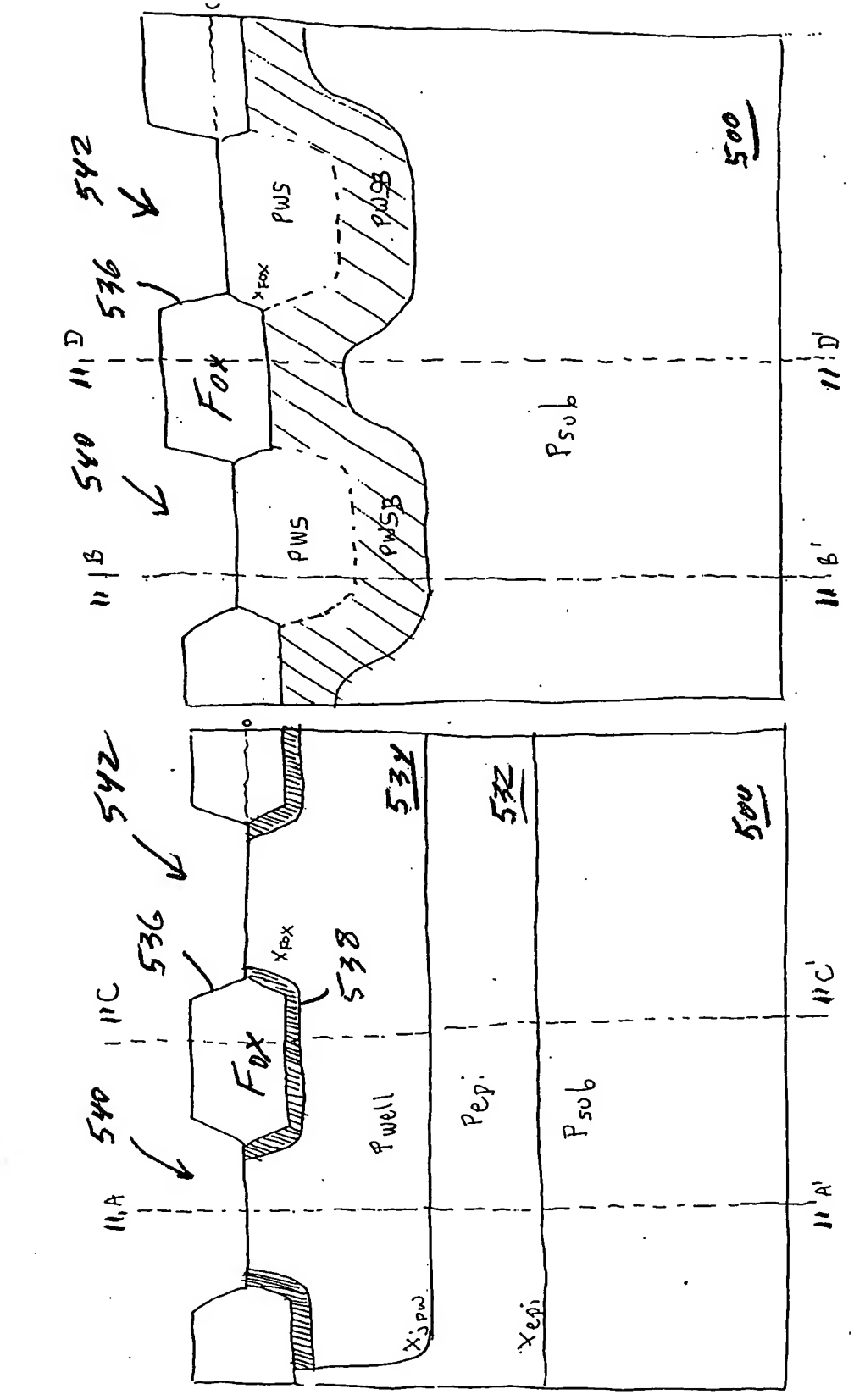


Fig. 11A

Fig. 11B

Fig. 11C

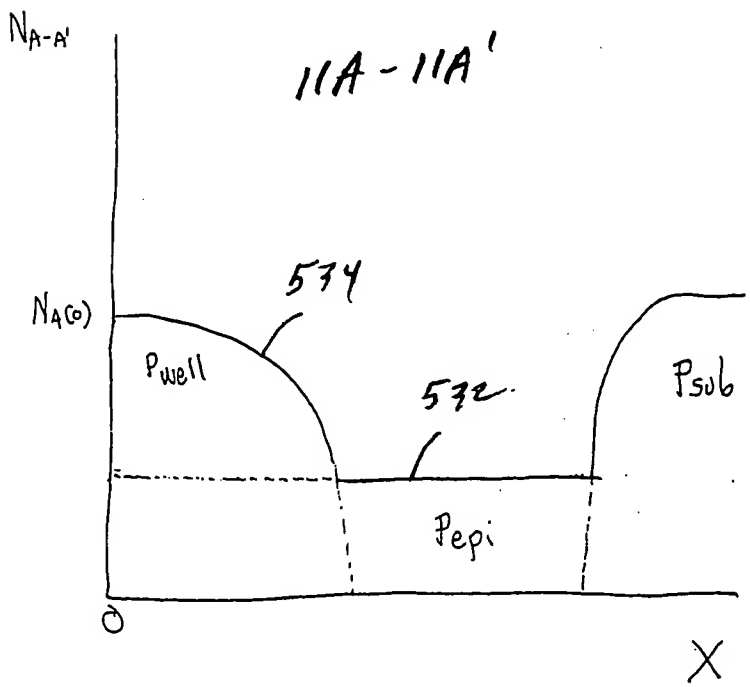


Fig. 11D

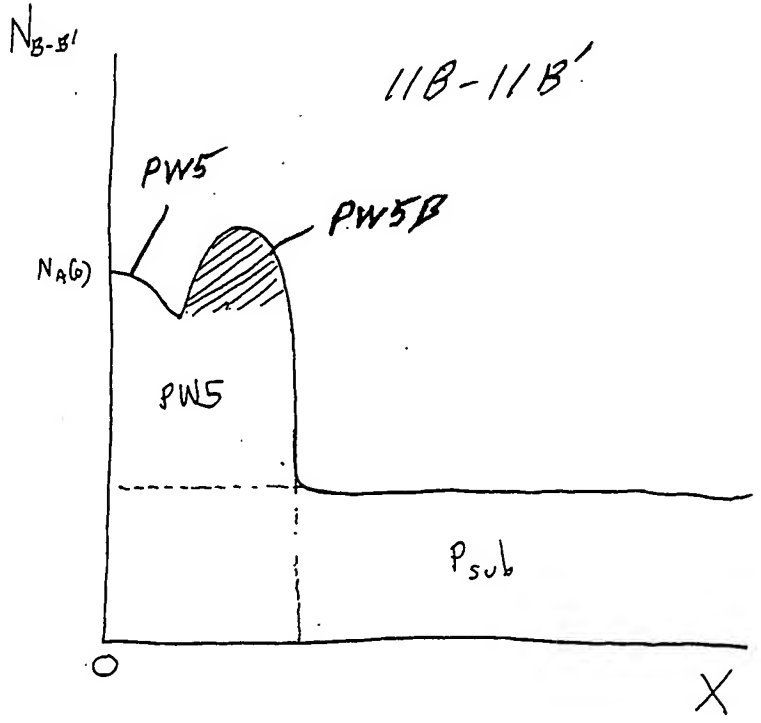


Fig. 11E

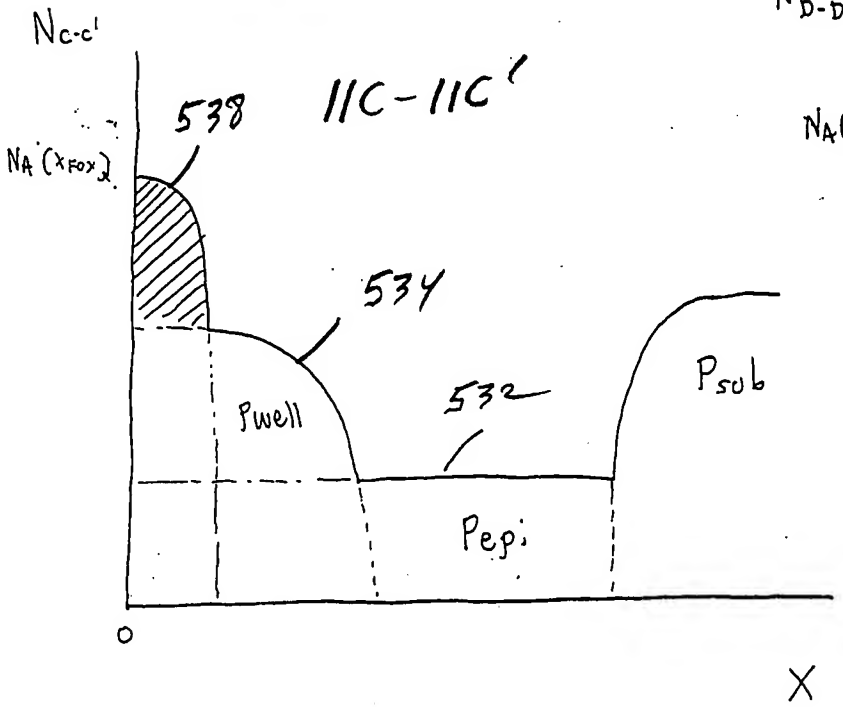


Fig. 11F

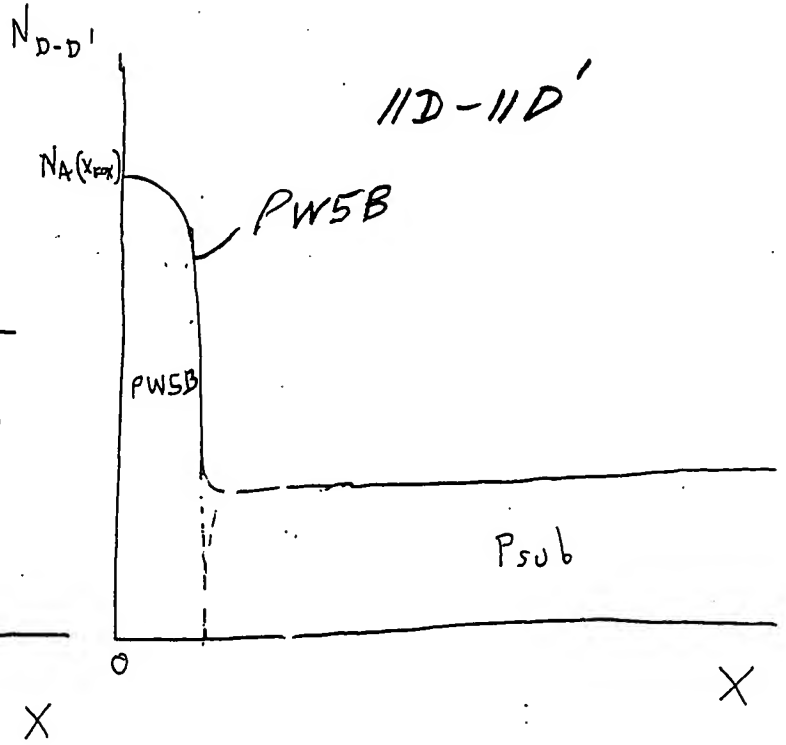


Fig. 11H

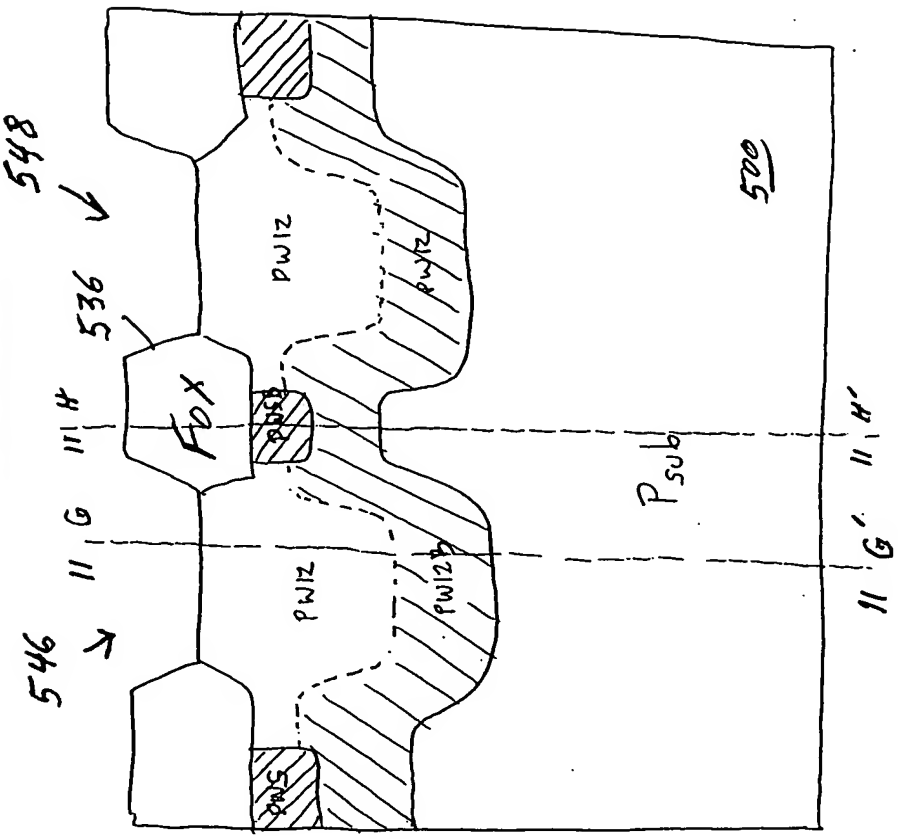


Fig. 11G

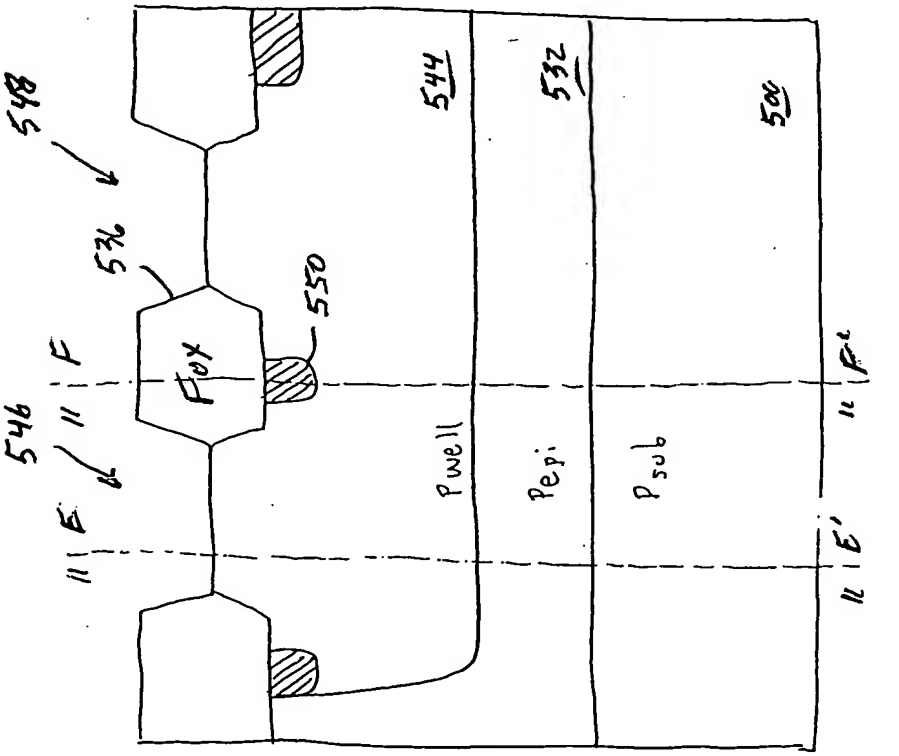


Fig. 11I

11E-11E'

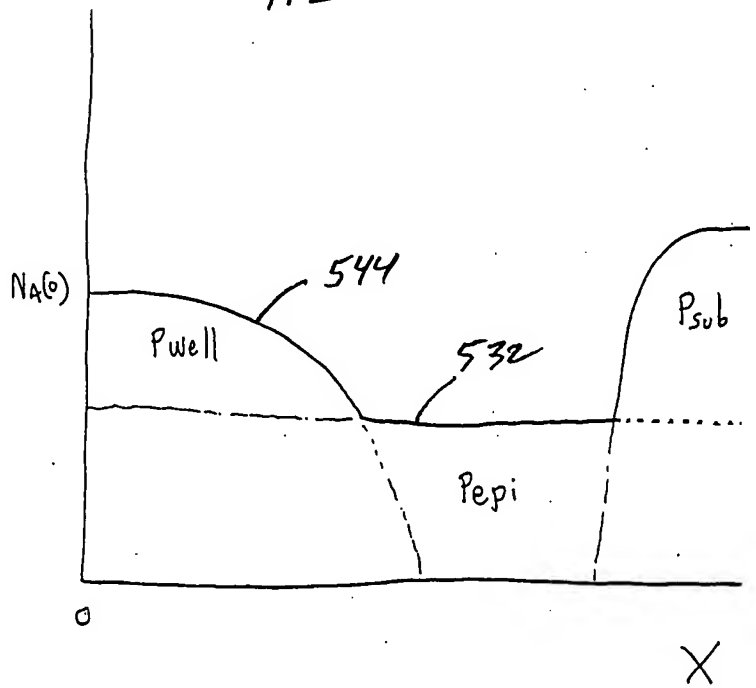


Fig. 11J

11G-11G'

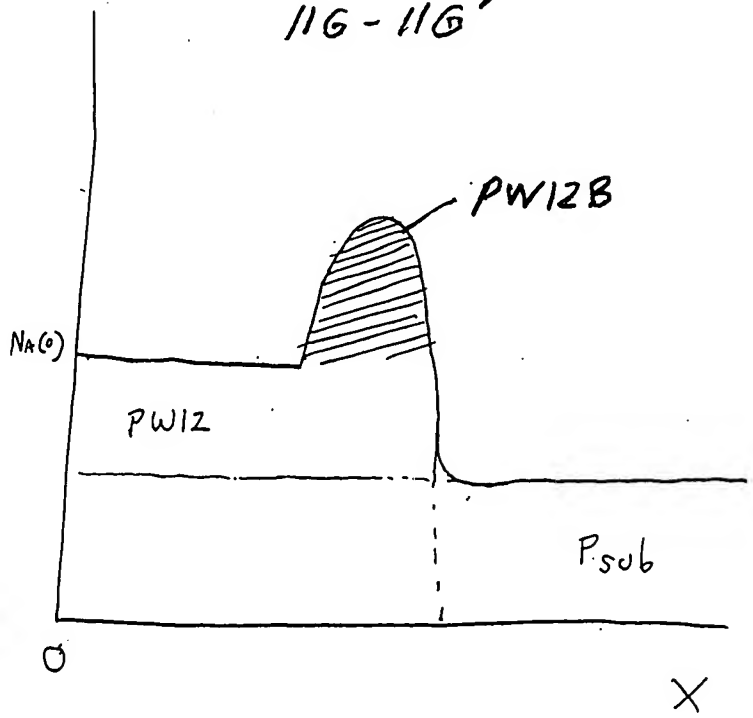


Fig. 11K

11F-11F'

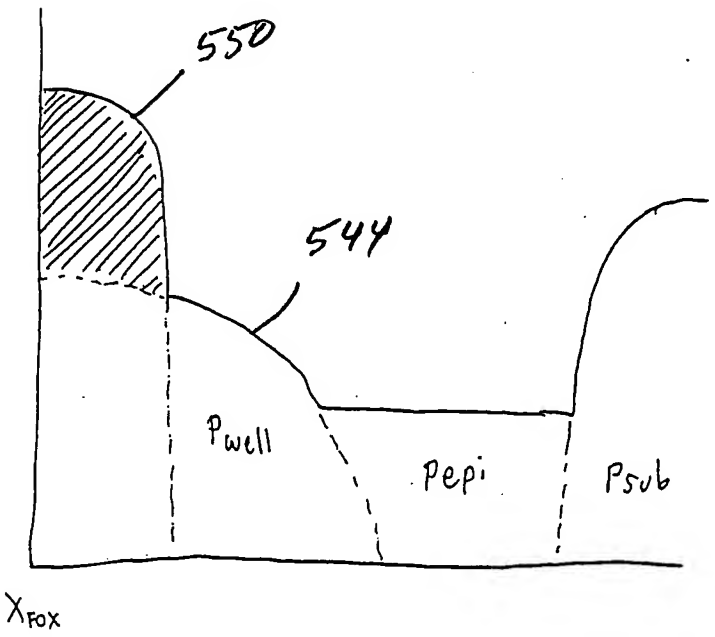


Fig. 11L

11H-11H'

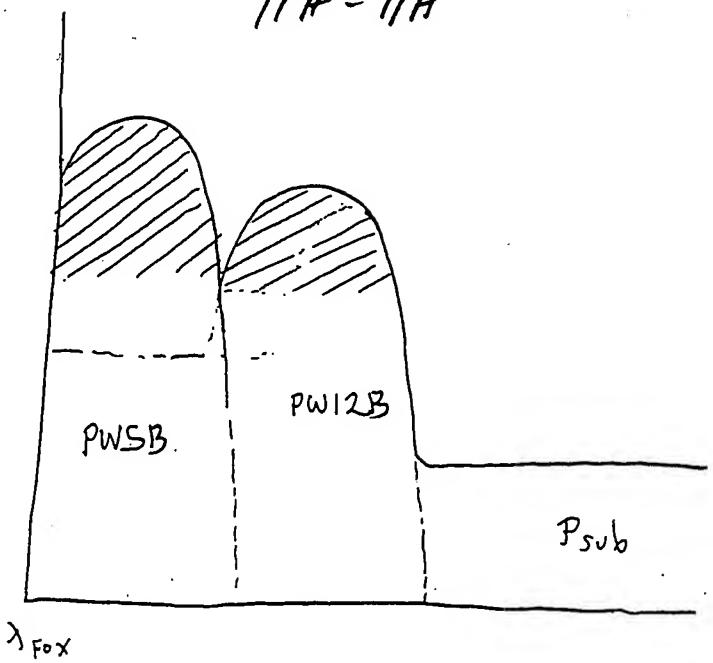


Fig. 12B

implanted

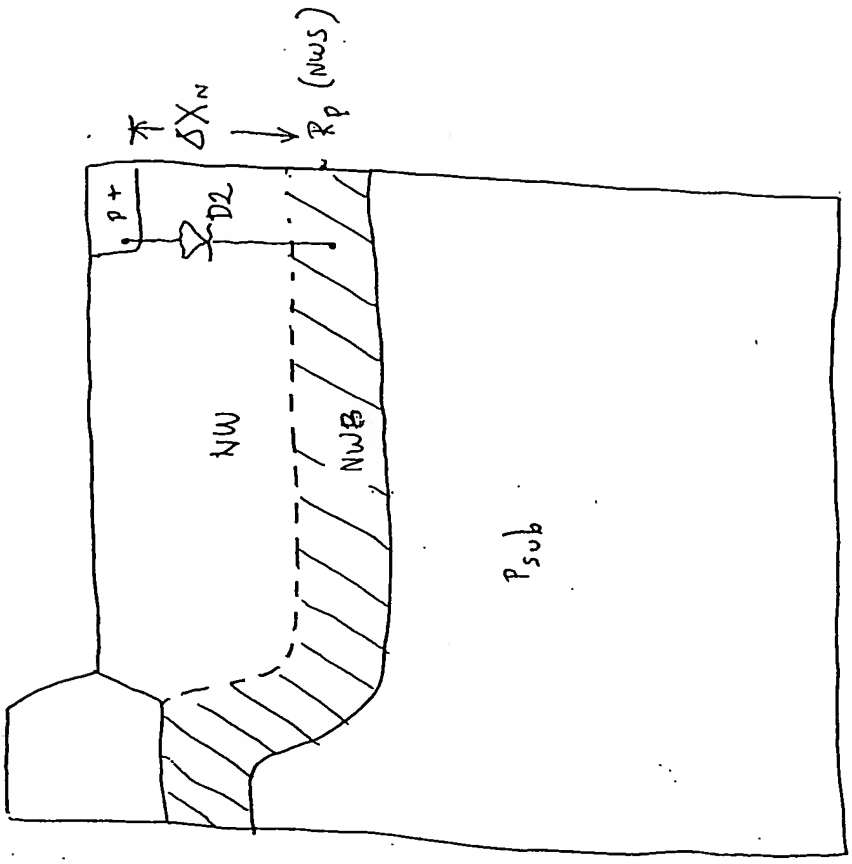


Fig. 12A

epitaxial

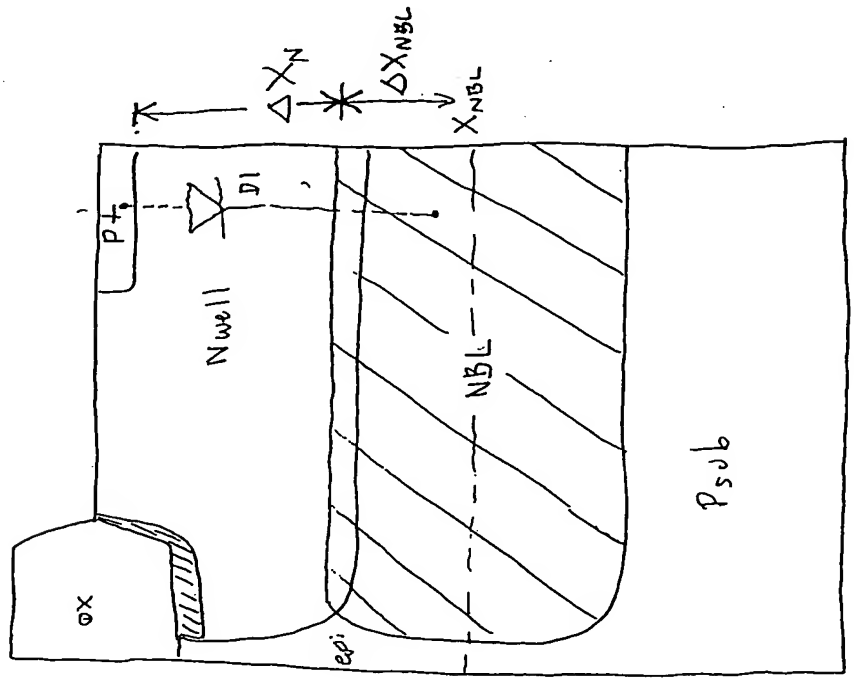


Fig. 12C

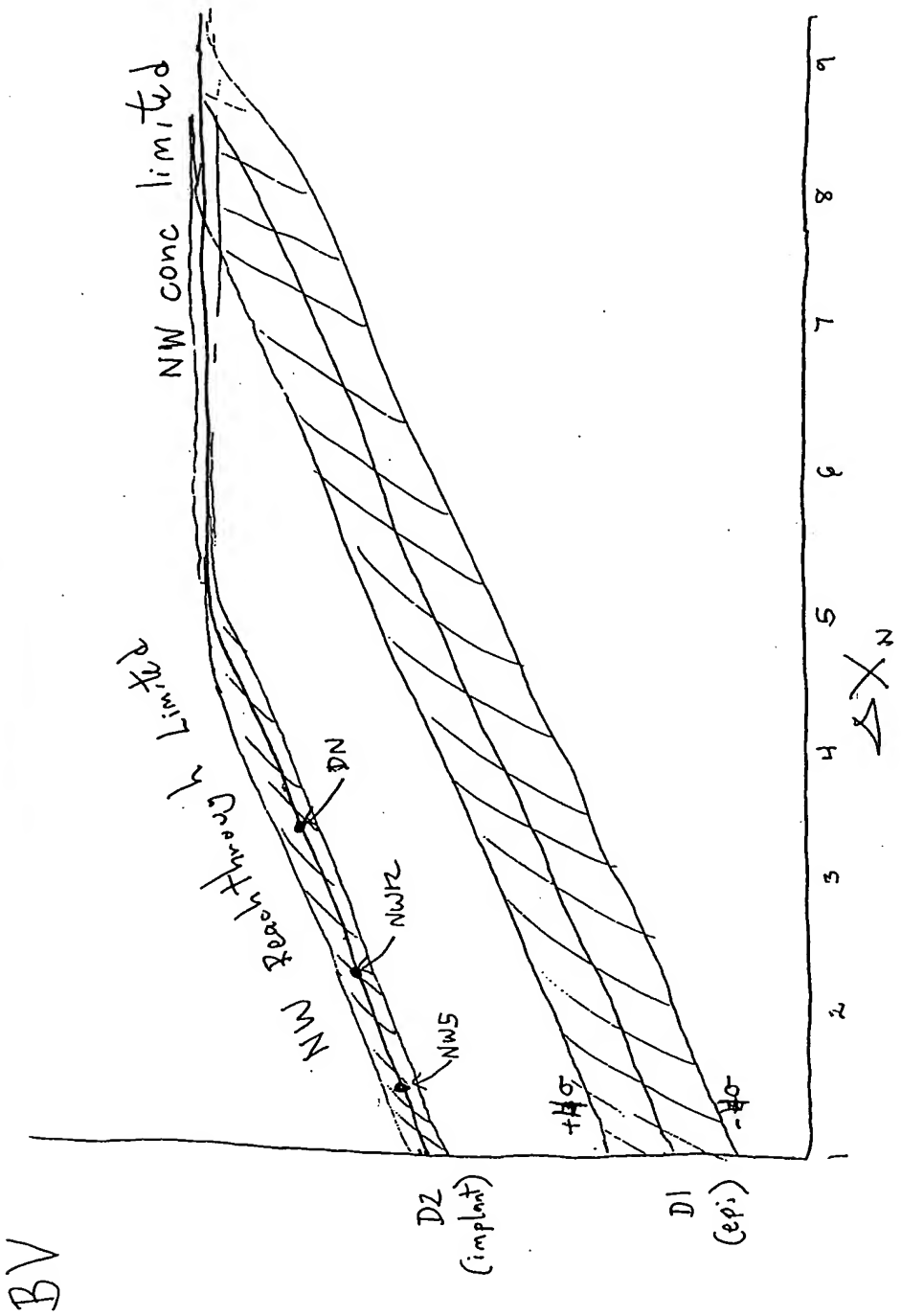

BV
D2
(implant)
D1
(epi)
NW Feedthrough
NW conc limited
DN
NW2
NW5
+Hσ
-Hσ
1
2
3
4
5
6
7
8
9
X

Fig. 13A

Prior Art

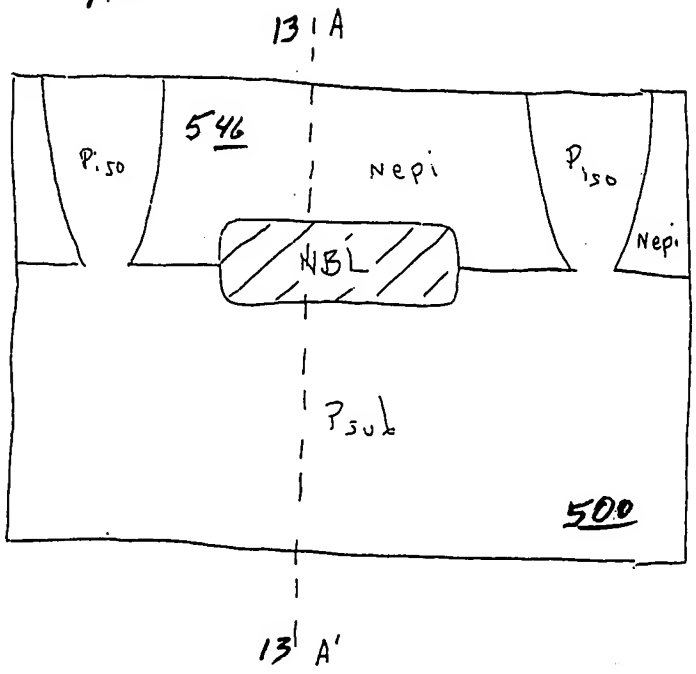


Fig. 13B

Prior Art

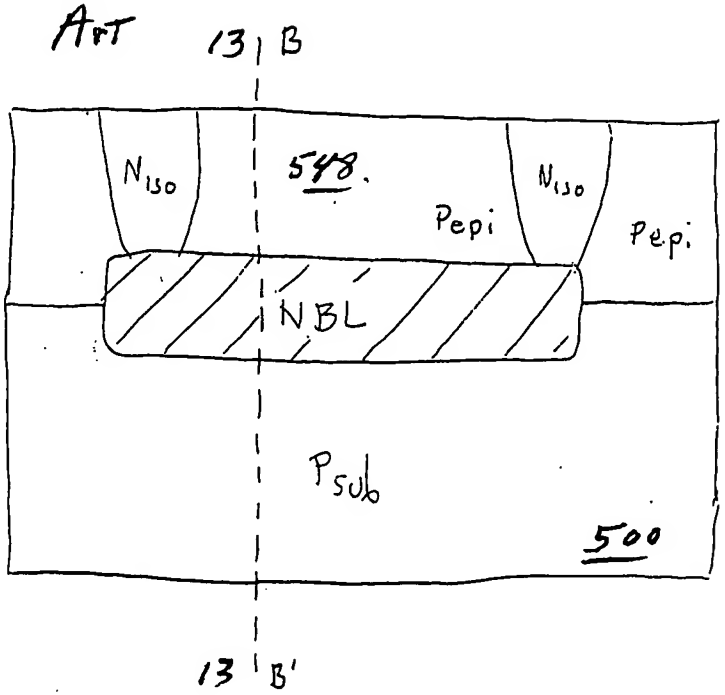


Fig 13C

13A-13A'

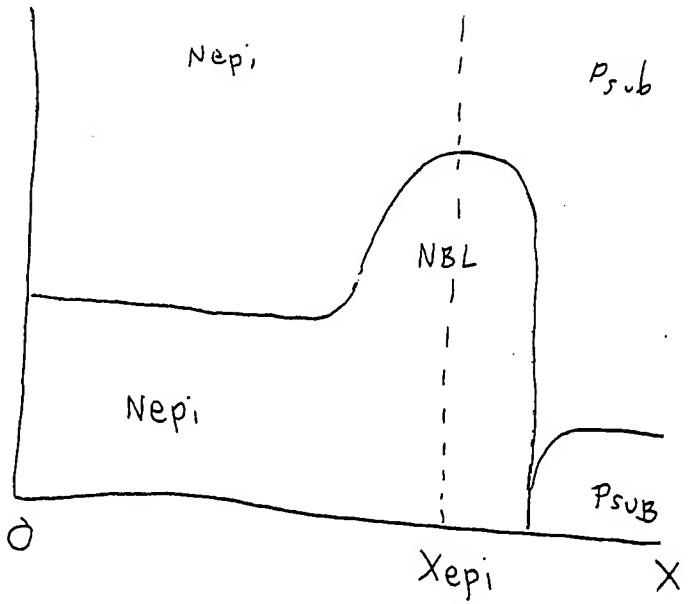


Fig 13D

13B - 13B'

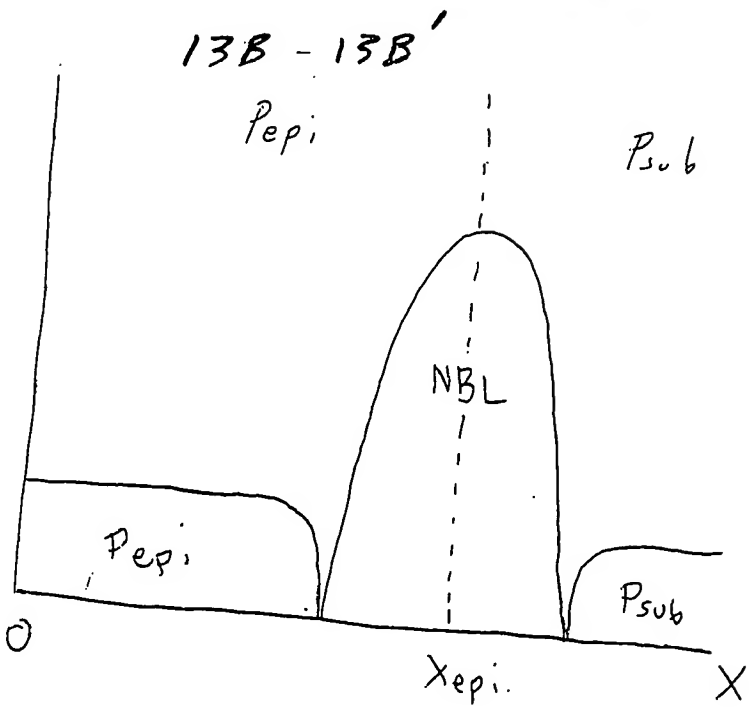


Fig. 13H

13D-13D'

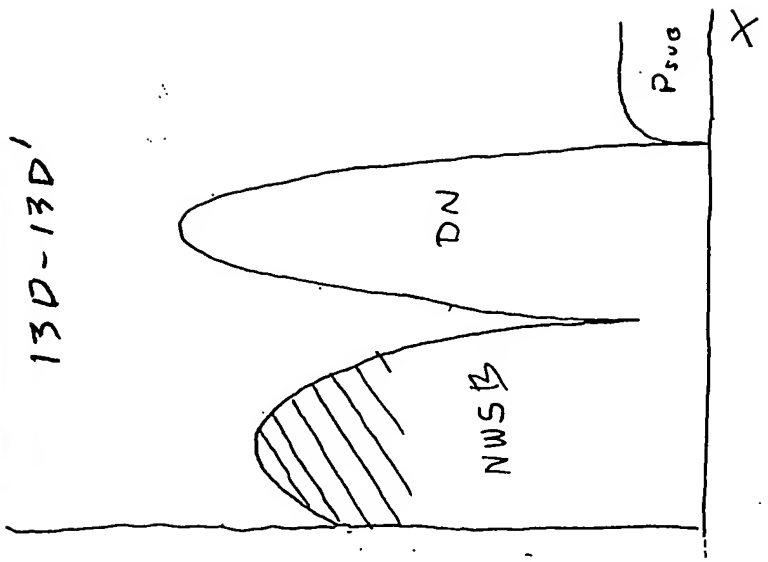
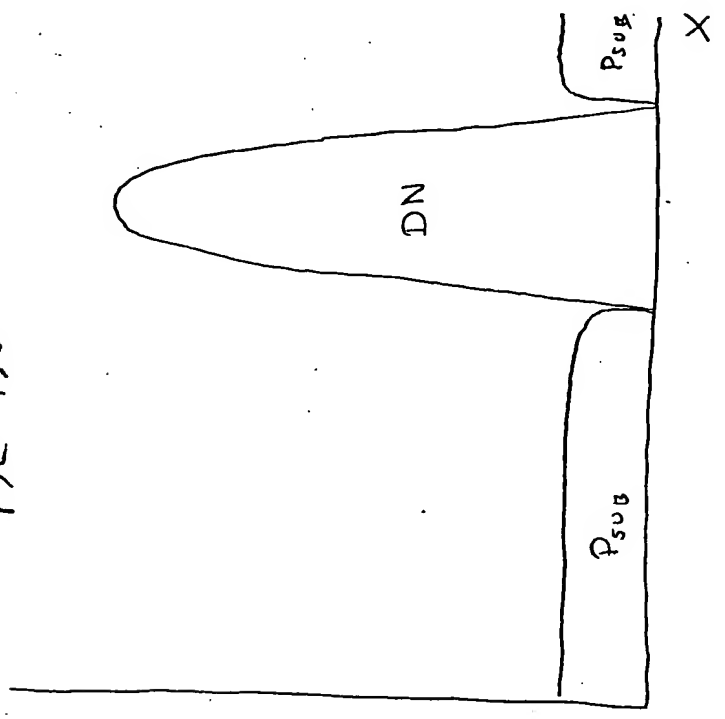


Fig. 13G

13C-13C'



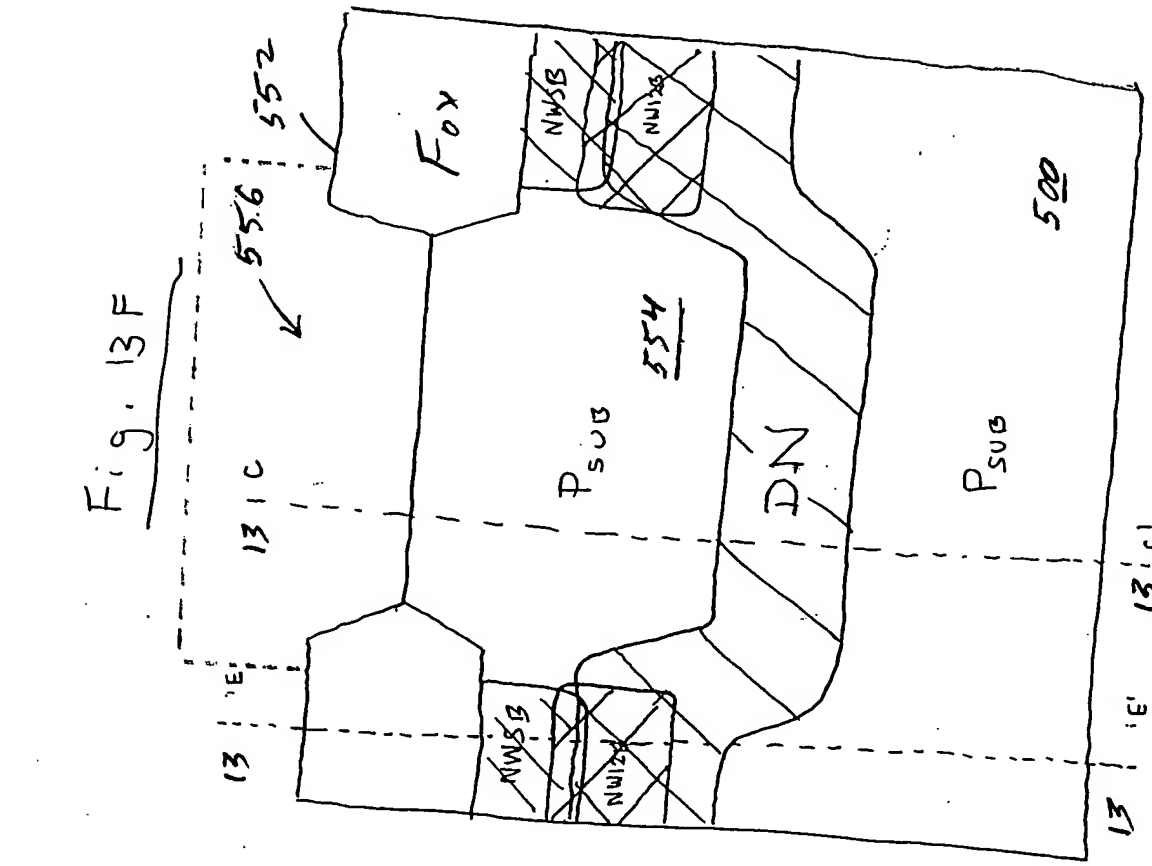


Fig. 13F
552
556
F_{OX}
NWSB
NWIN
554
P_{SUB}
DN
500
13
13'
13 'C
13 'E
13 'E'
13 'C'

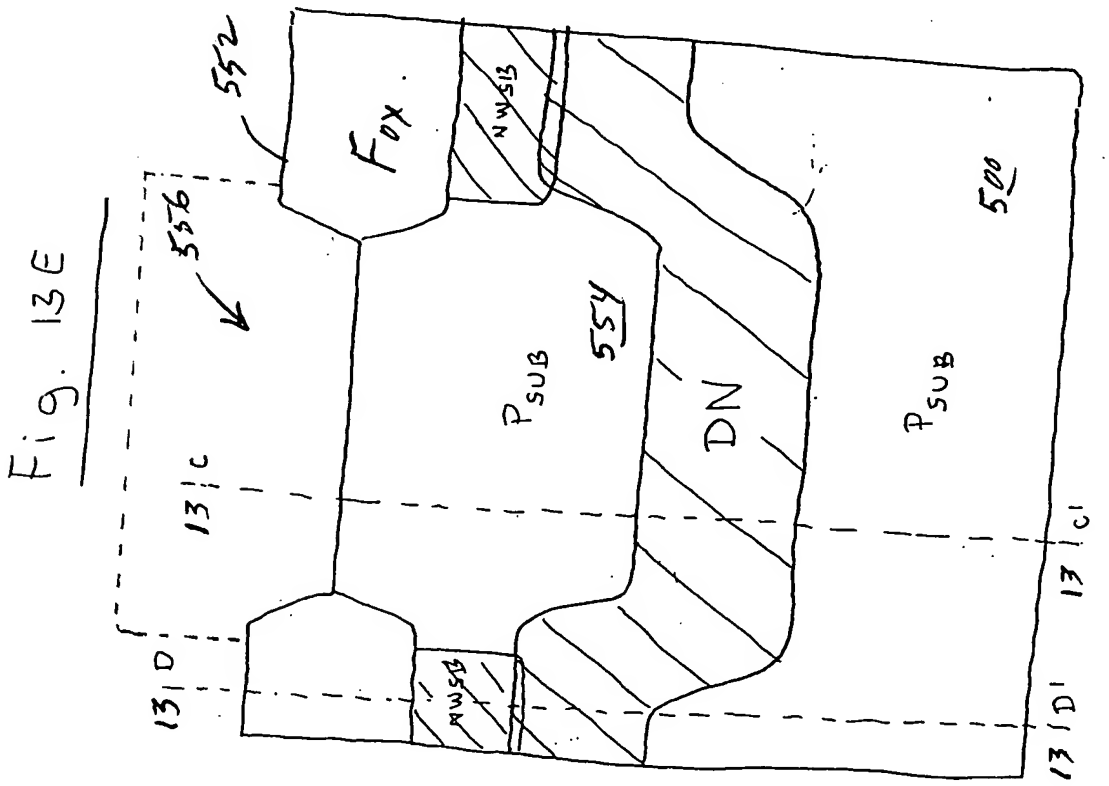
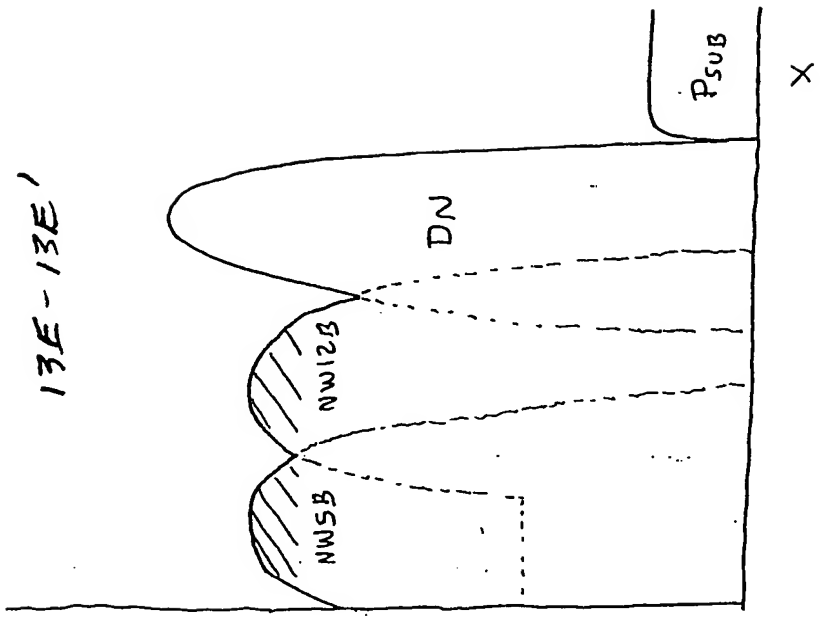


Fig. 13E
552
556
F_{OX}
NWSB
554
P_{SUB}
DN
500
13
13'
13 'C
13 'C'
13 'D
13 'D'

Fig. 13I

13E-13E'



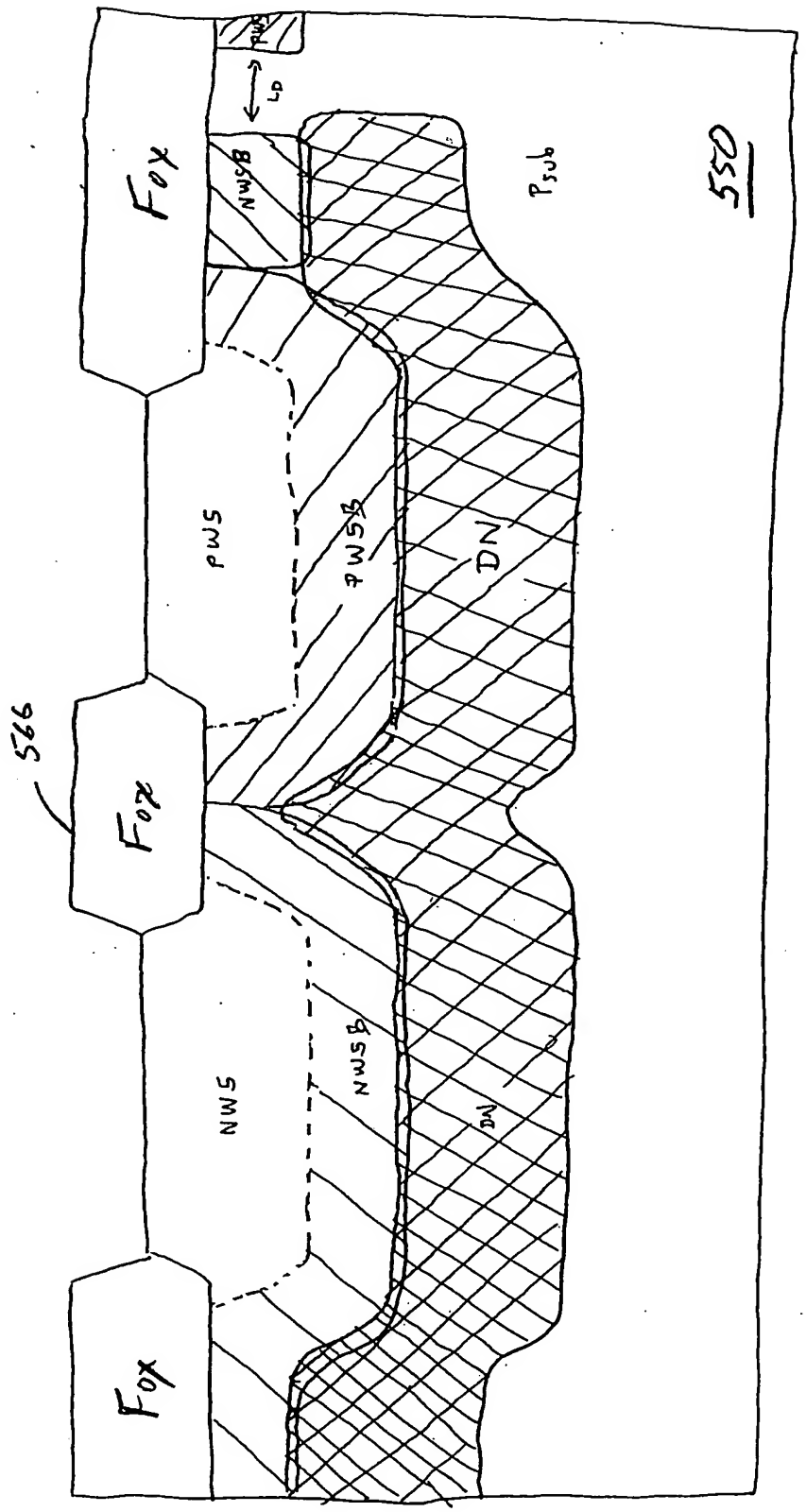


Fig 14A

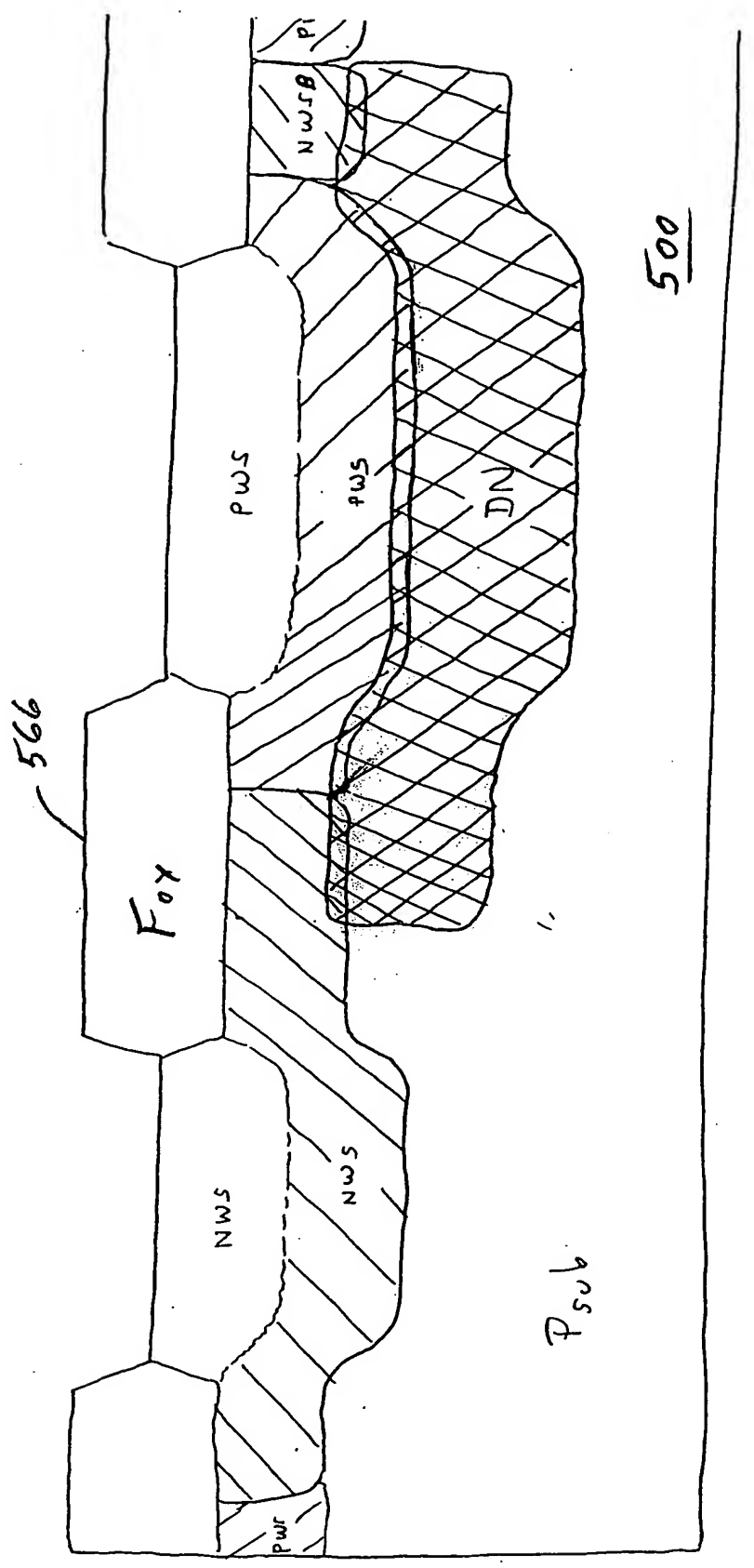


Fig. 14B

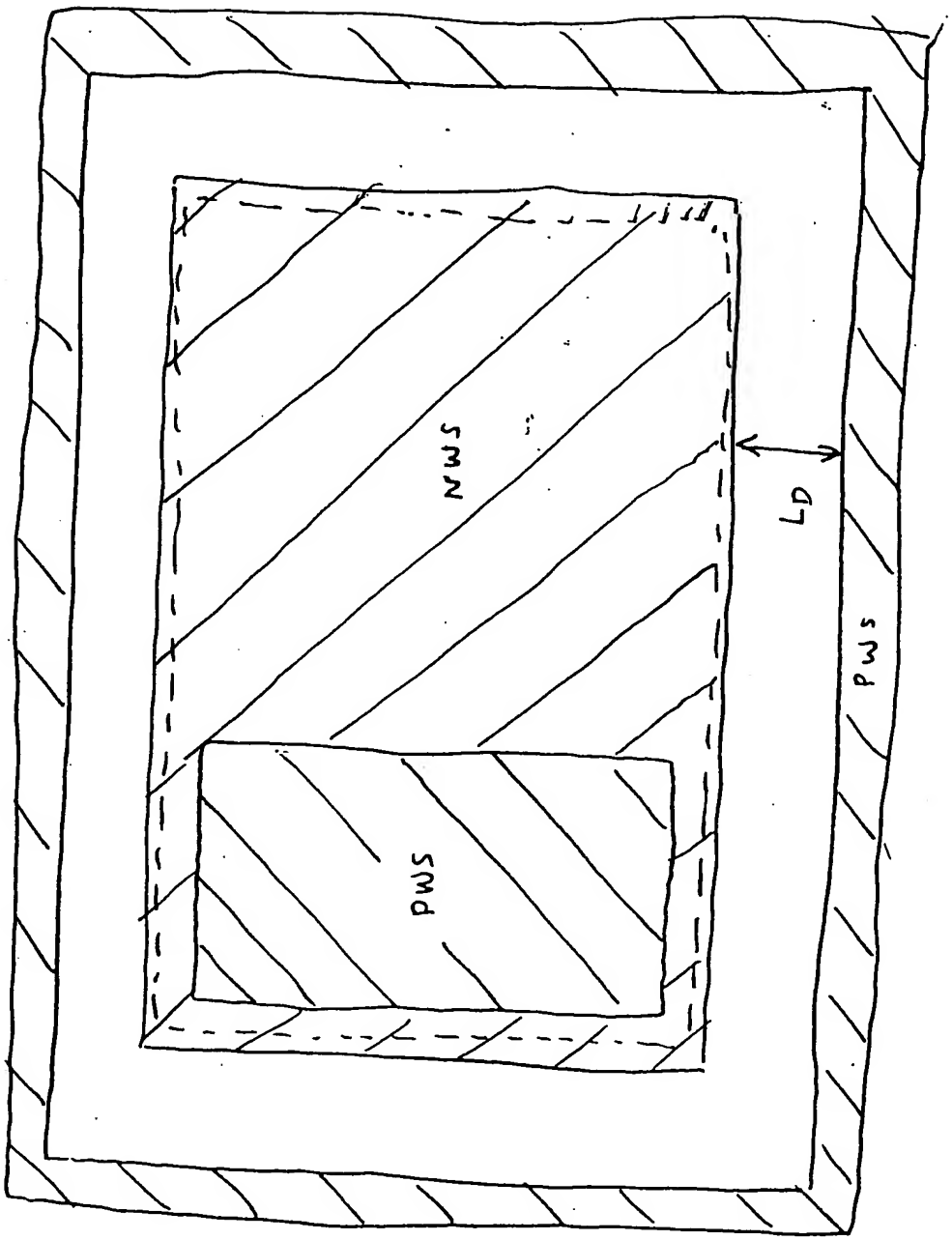


Fig. 14C

Fig. 14E

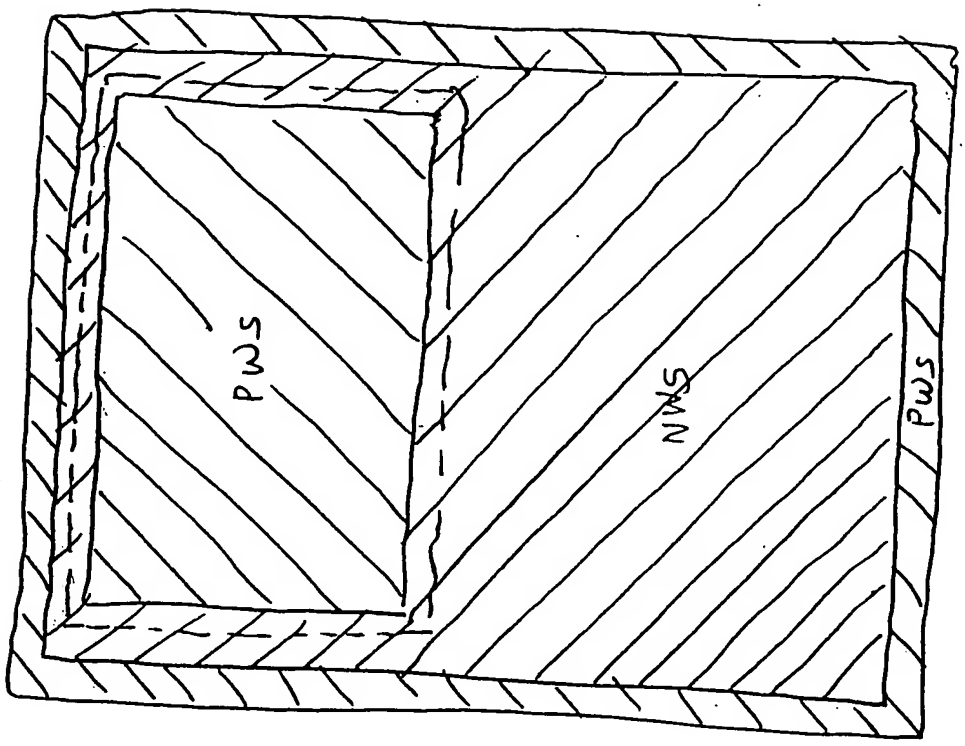
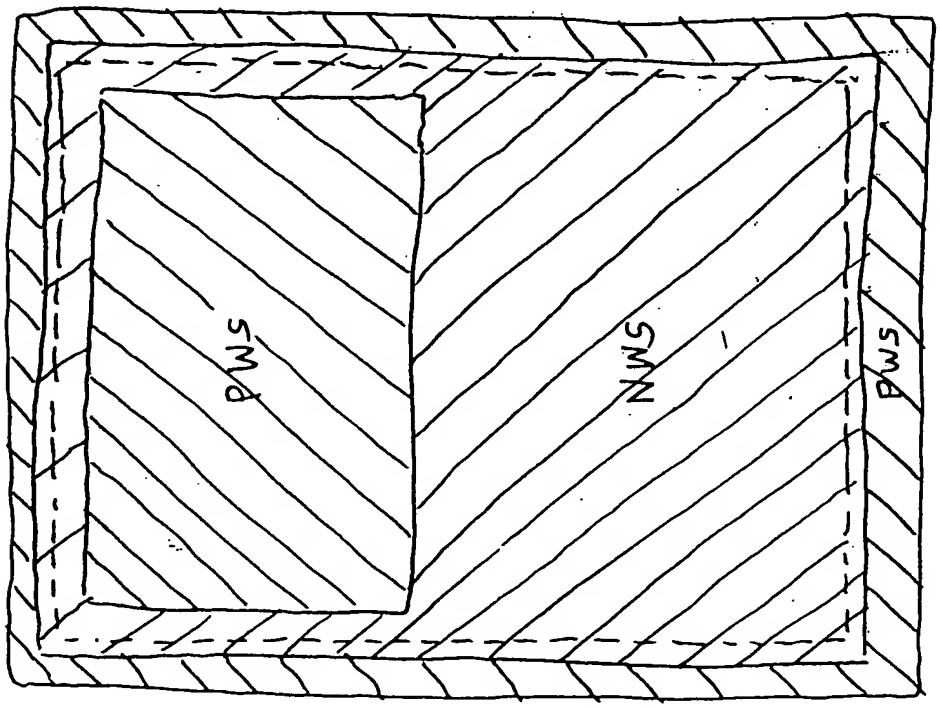


Fig 14D



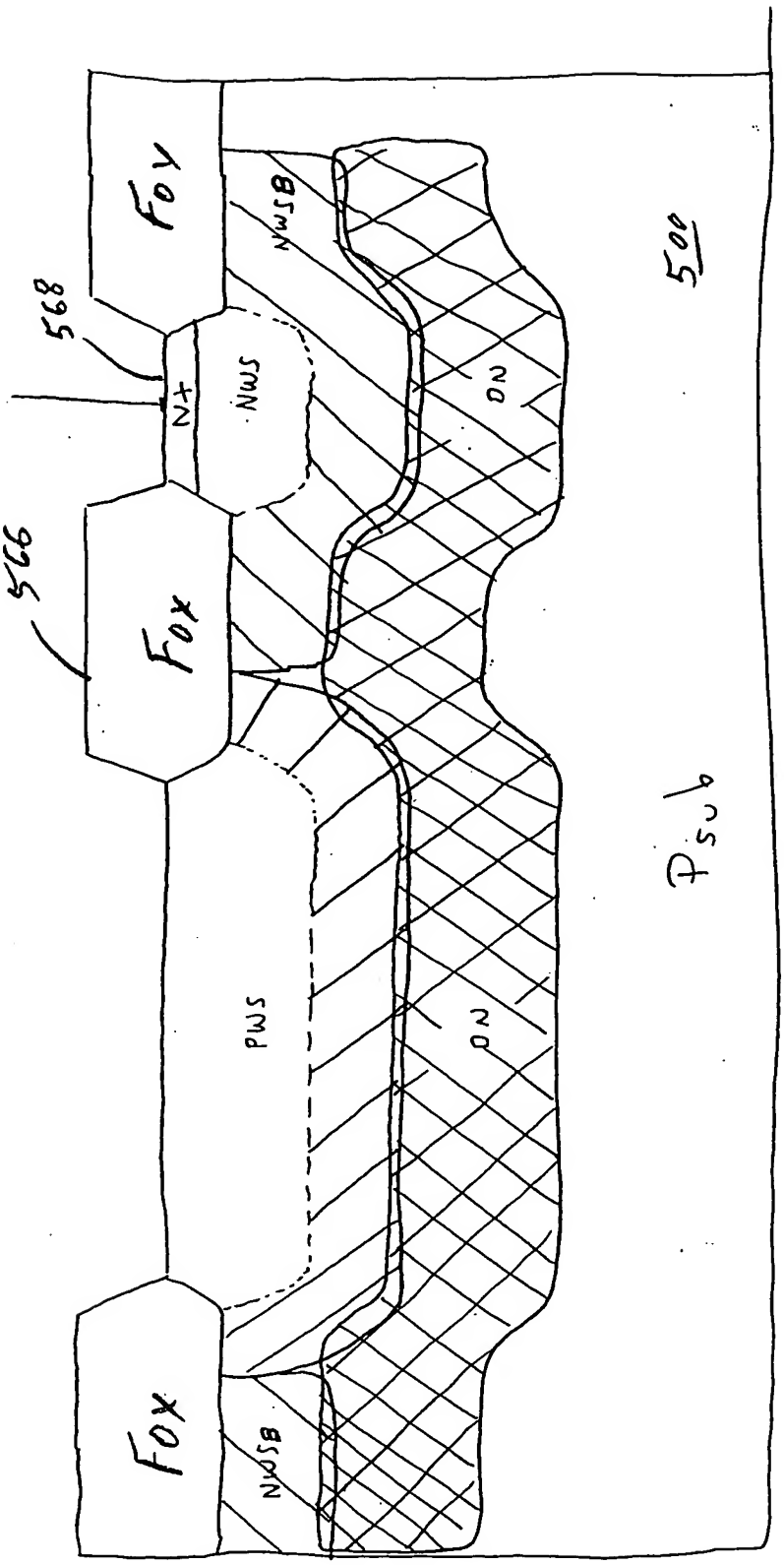

FOV
568
isolation
N+
NWS
NWSB
ON
500
566
FOX
PWS
ON
FOX
NWSB
Psub

Fig. 14F

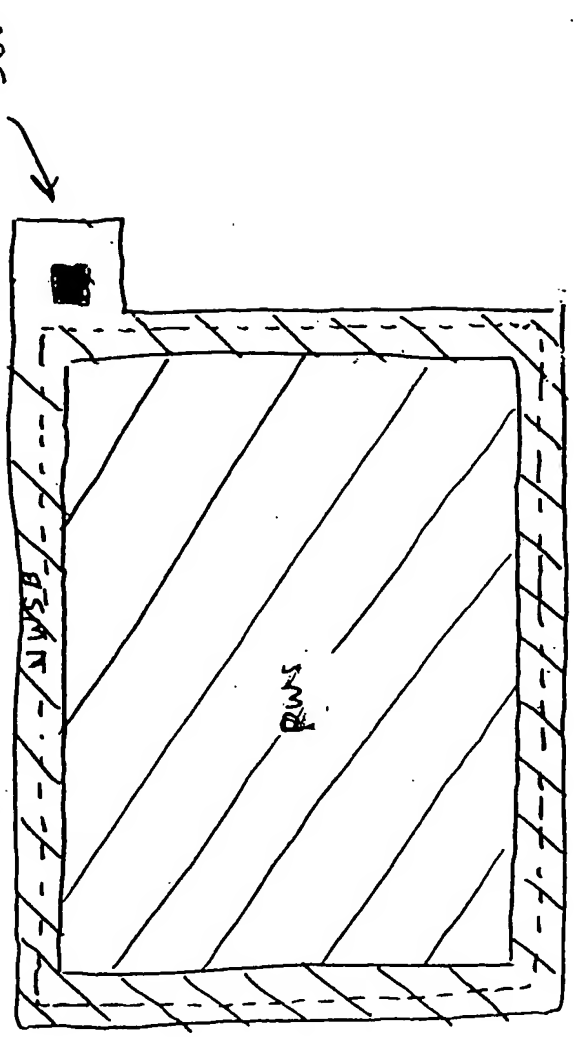


Fig. 146

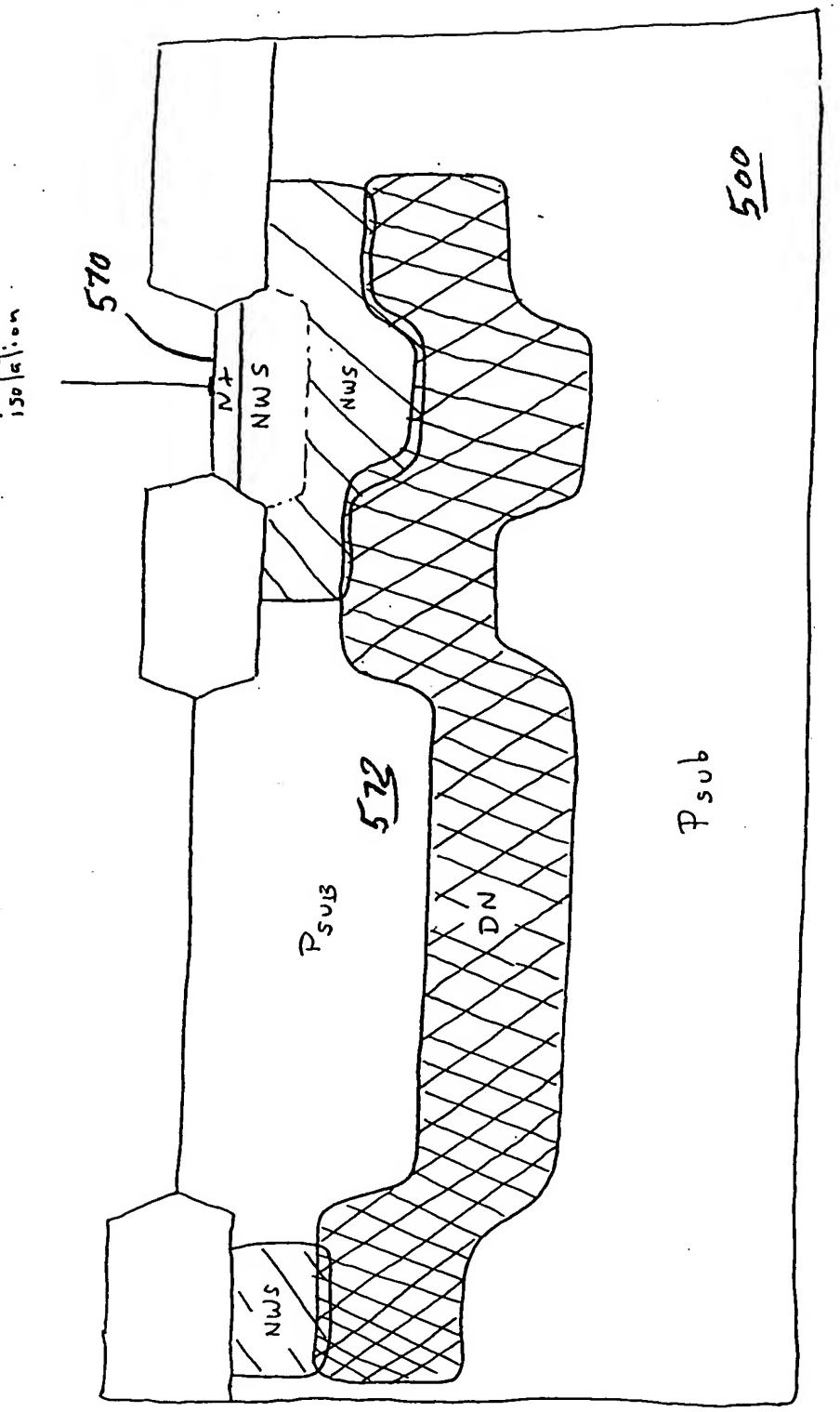


Fig. 14H

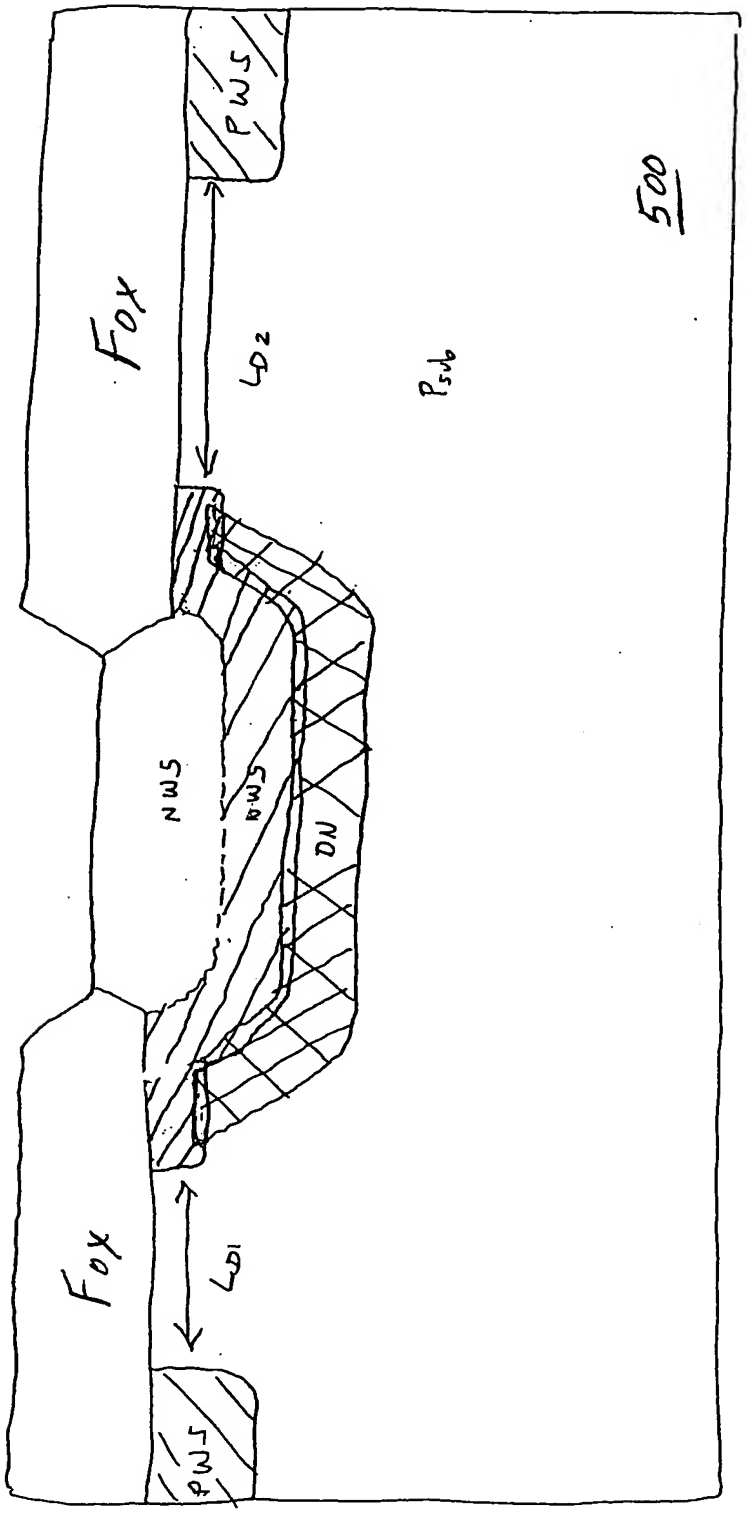


Fig. 14I

Fig. 14J

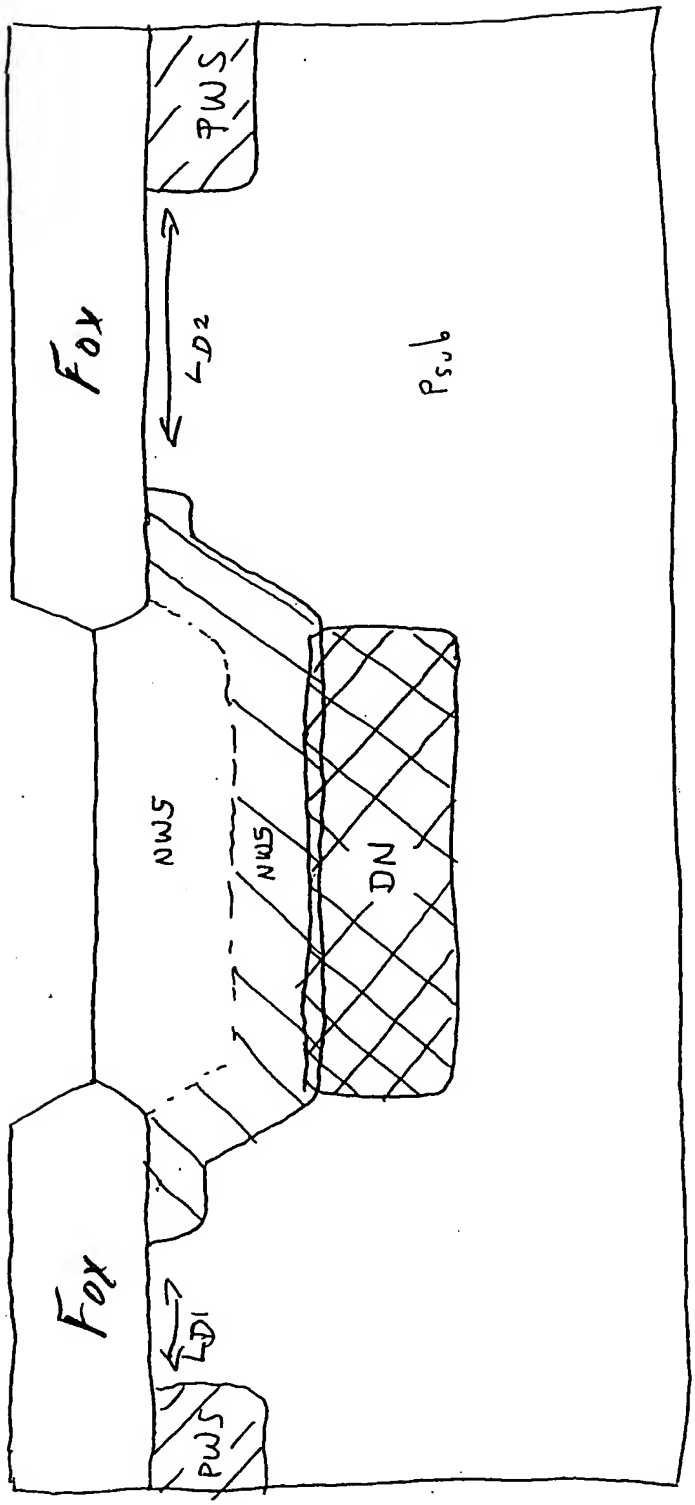


Fig. 14K

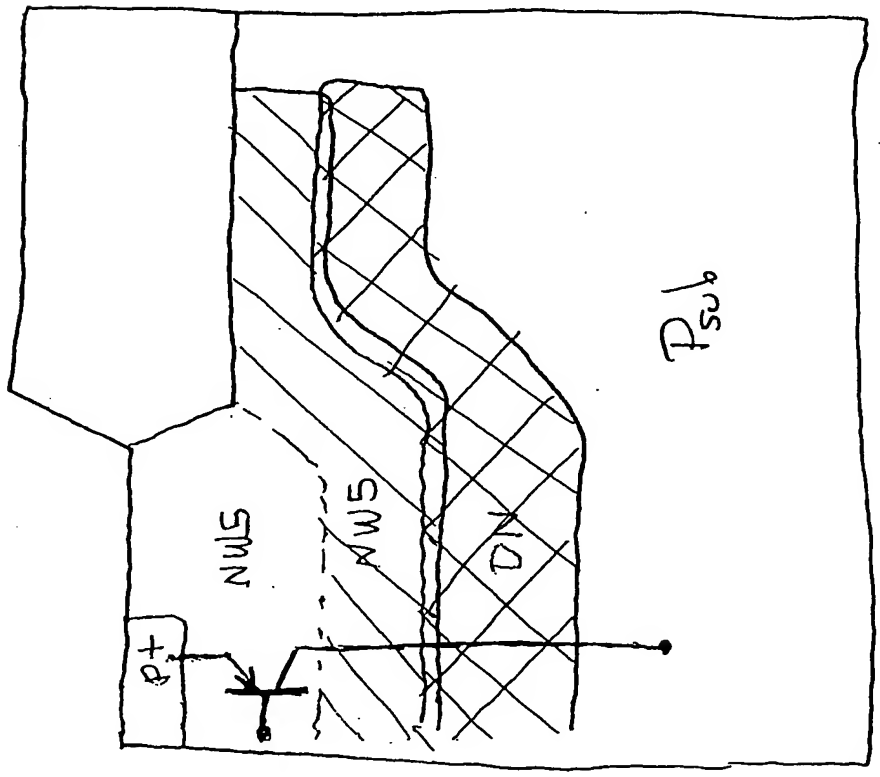
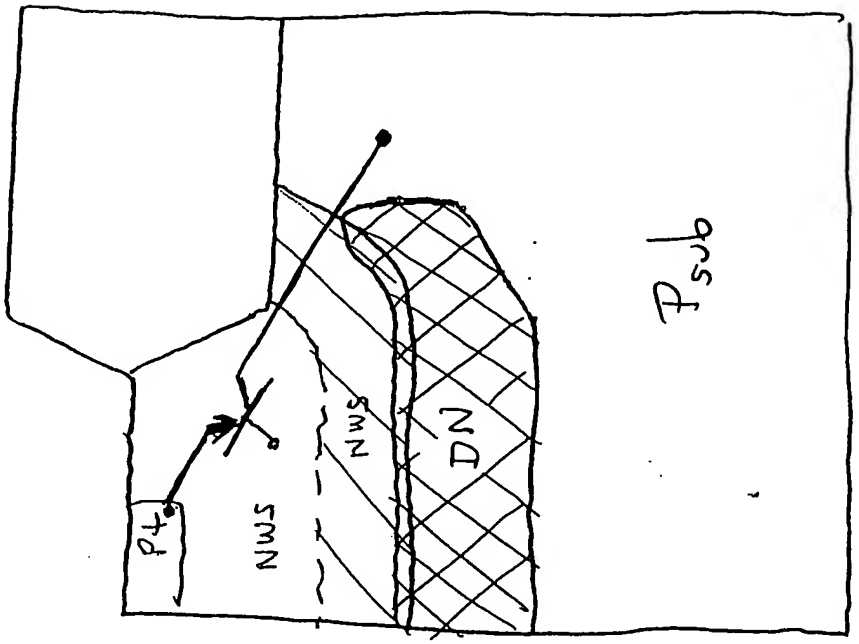


Fig. 14L



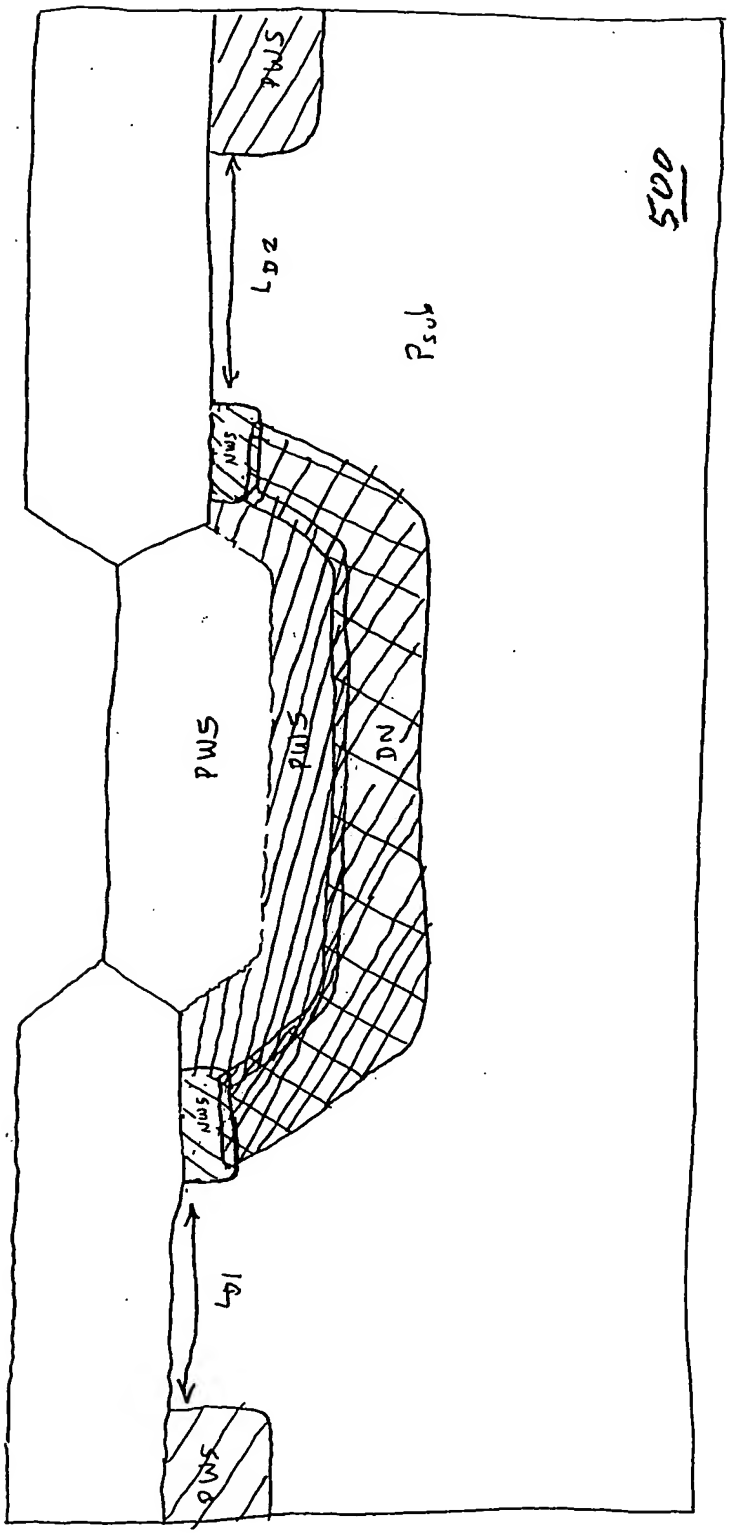


Fig. 14M

Fig. 14N

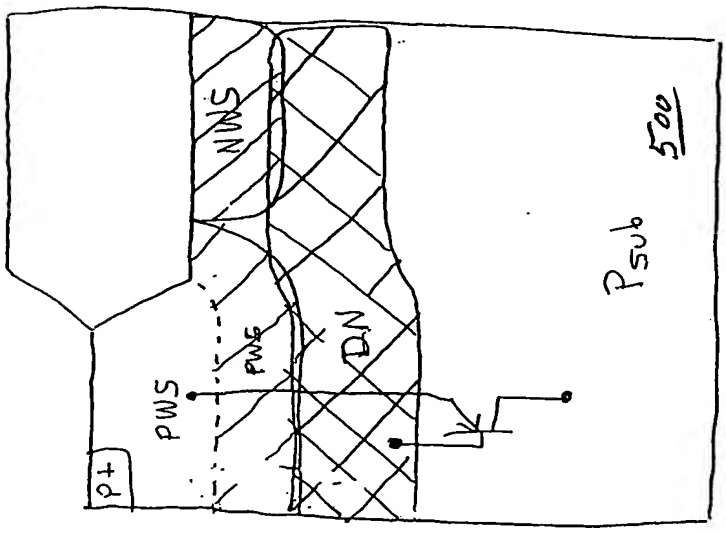


Fig. 14O

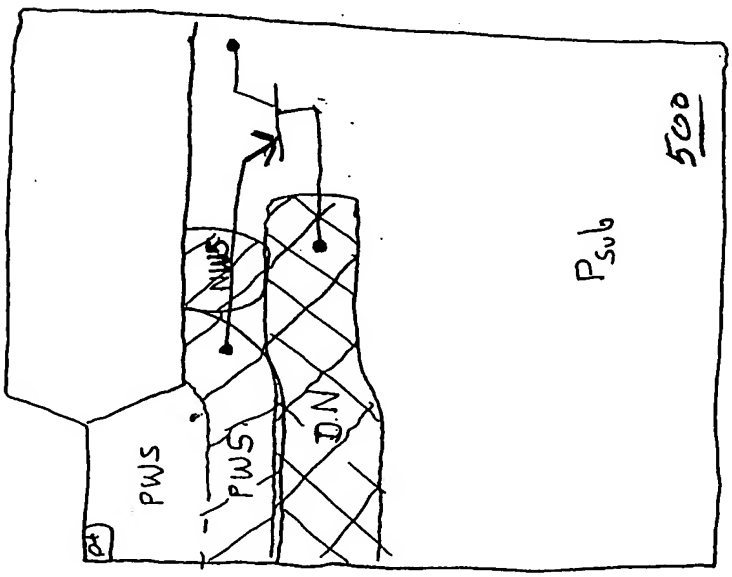
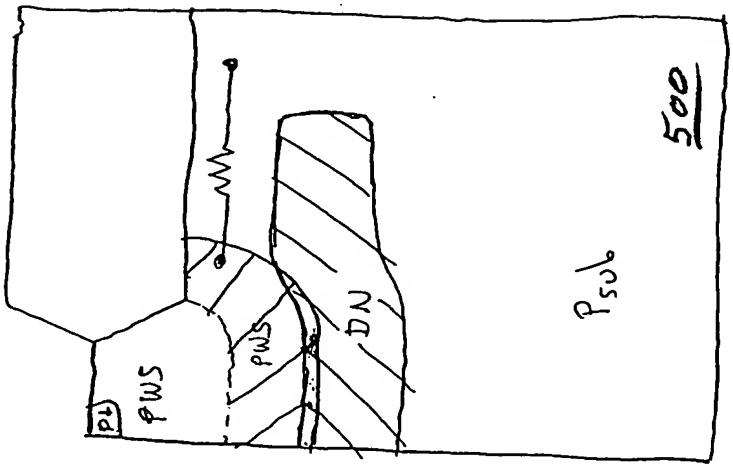


Fig. 14P



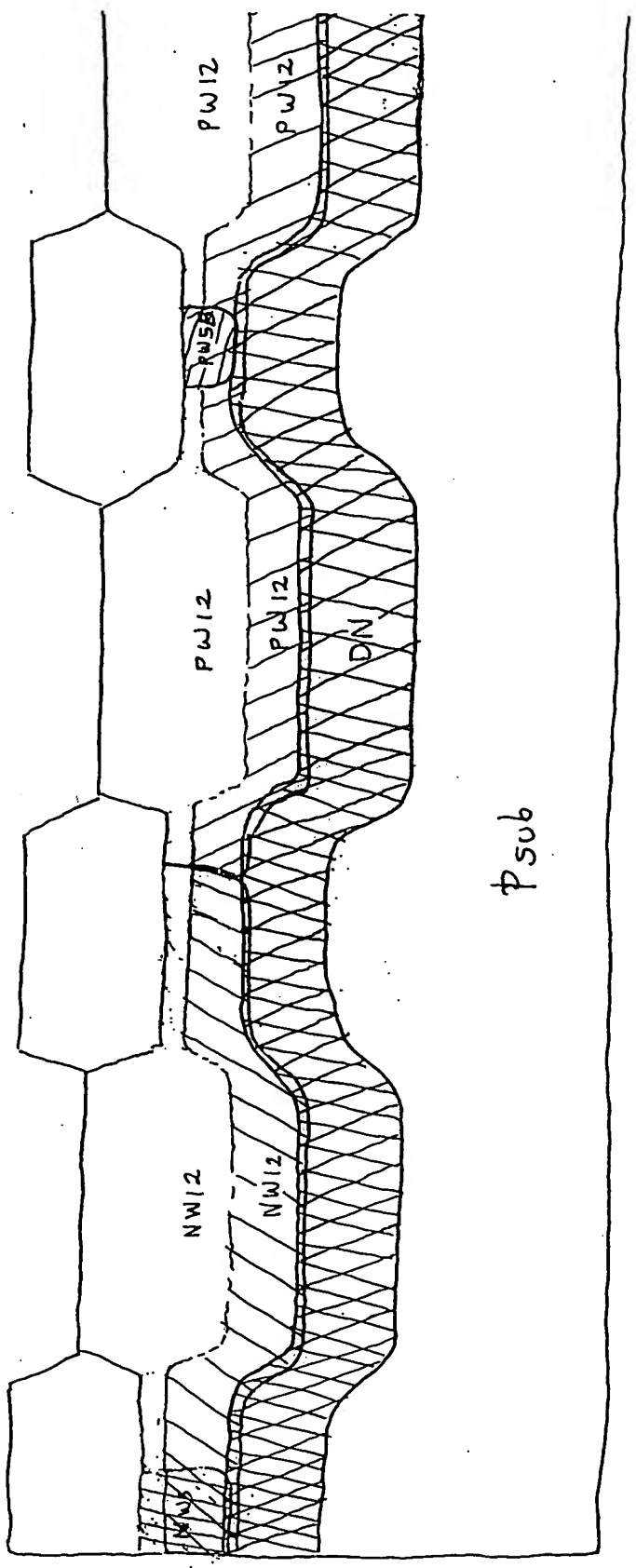


Fig. 15A

Fig, 15B

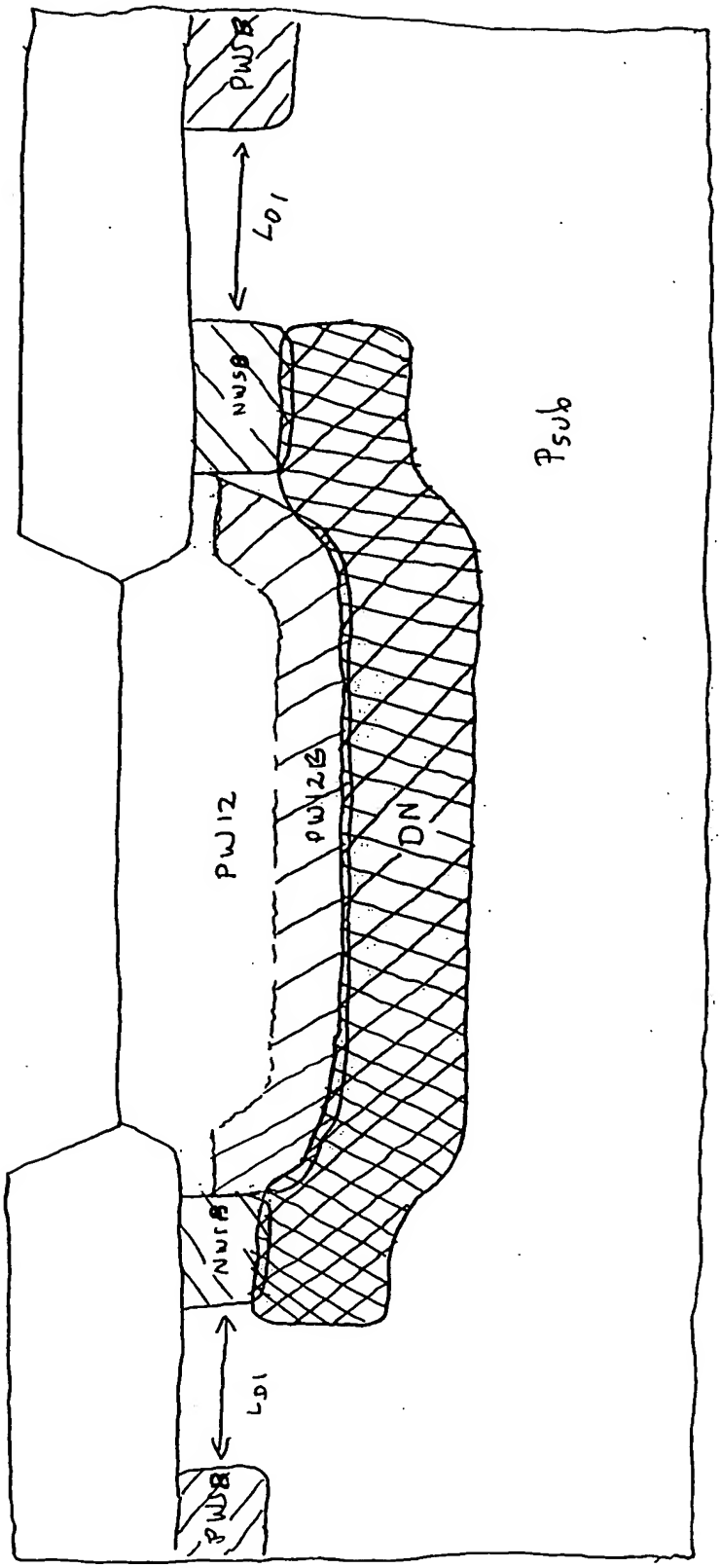
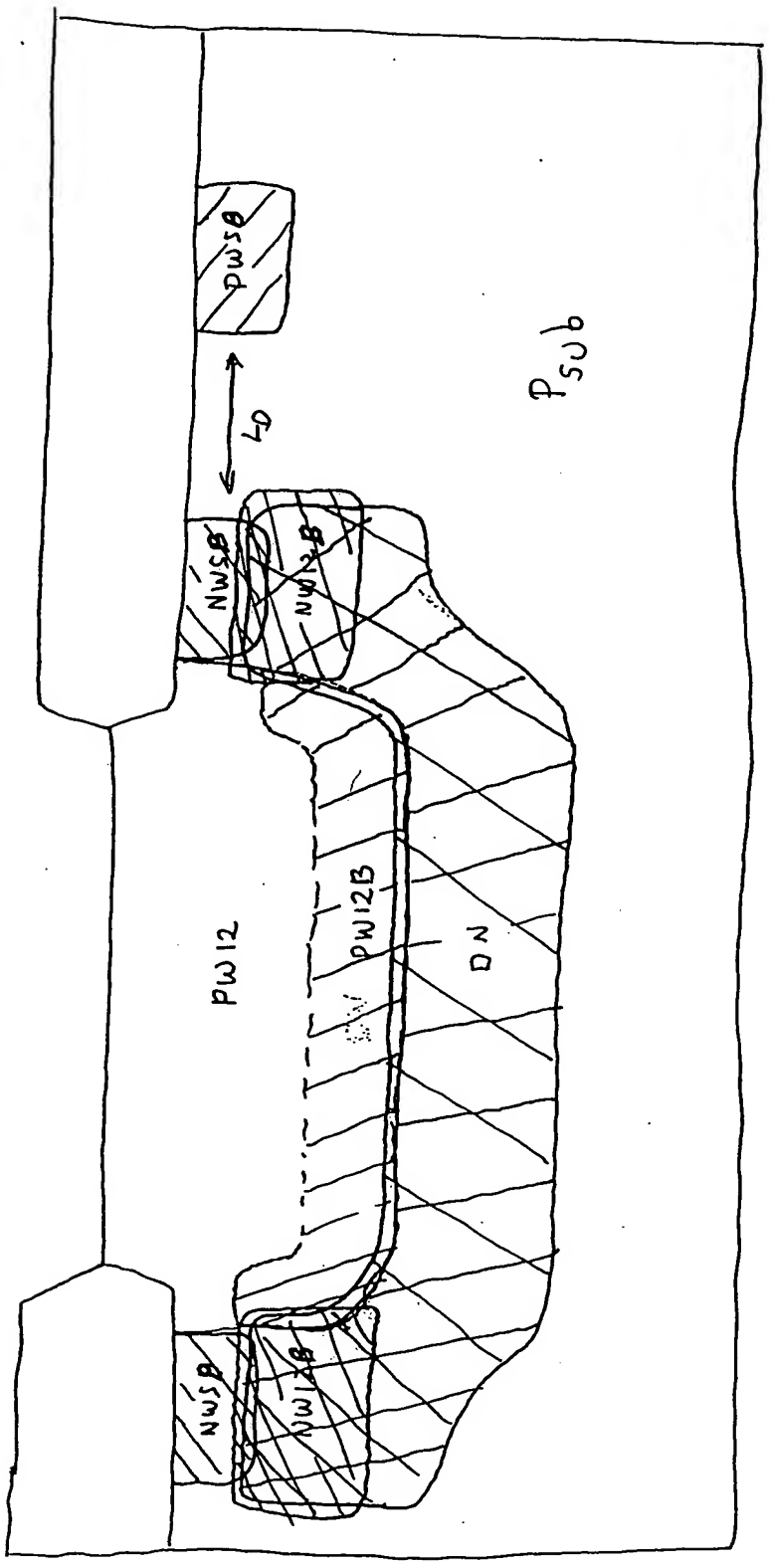


Fig. 15C



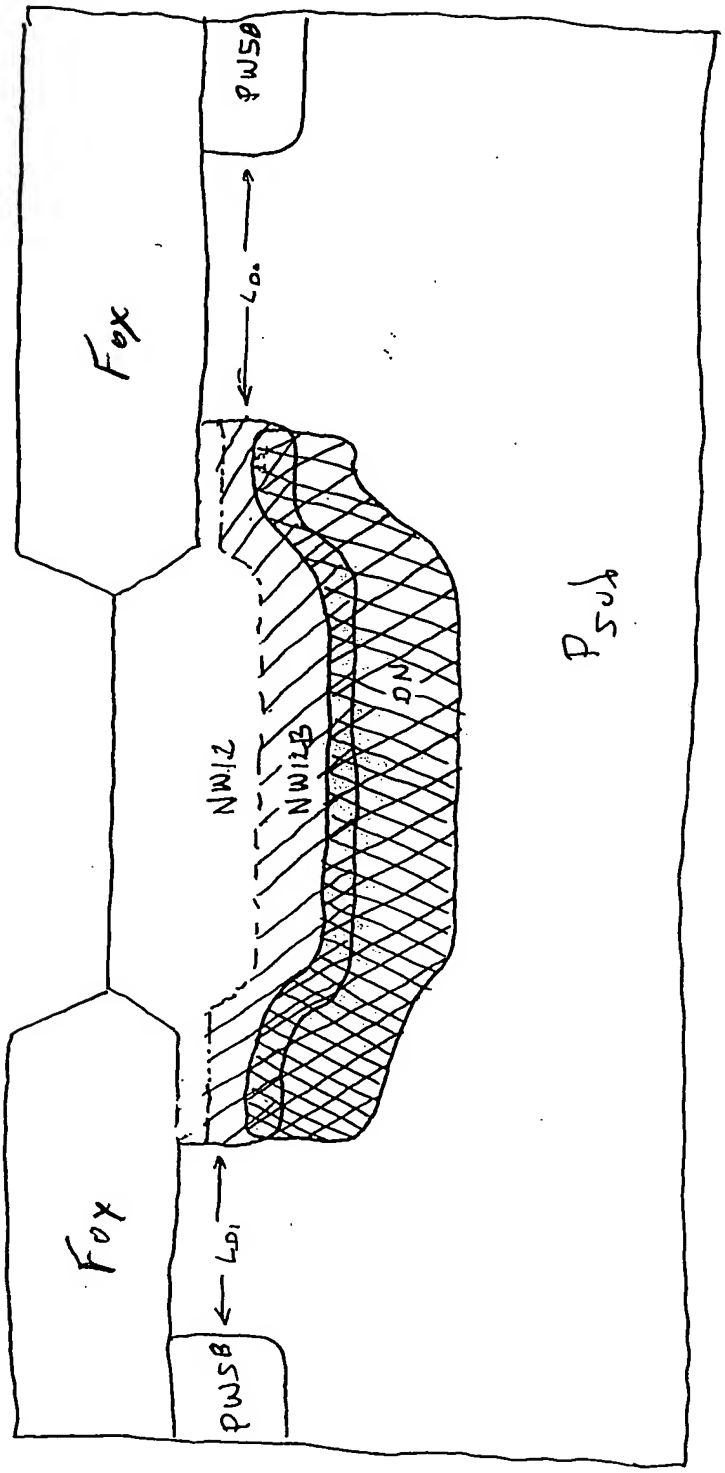


Fig. 15D

Fig. 15F

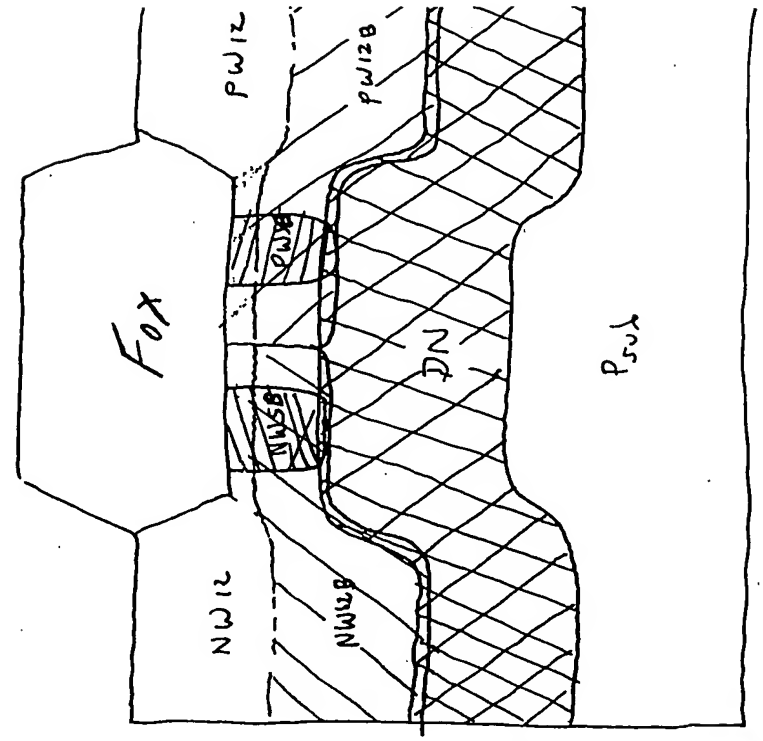
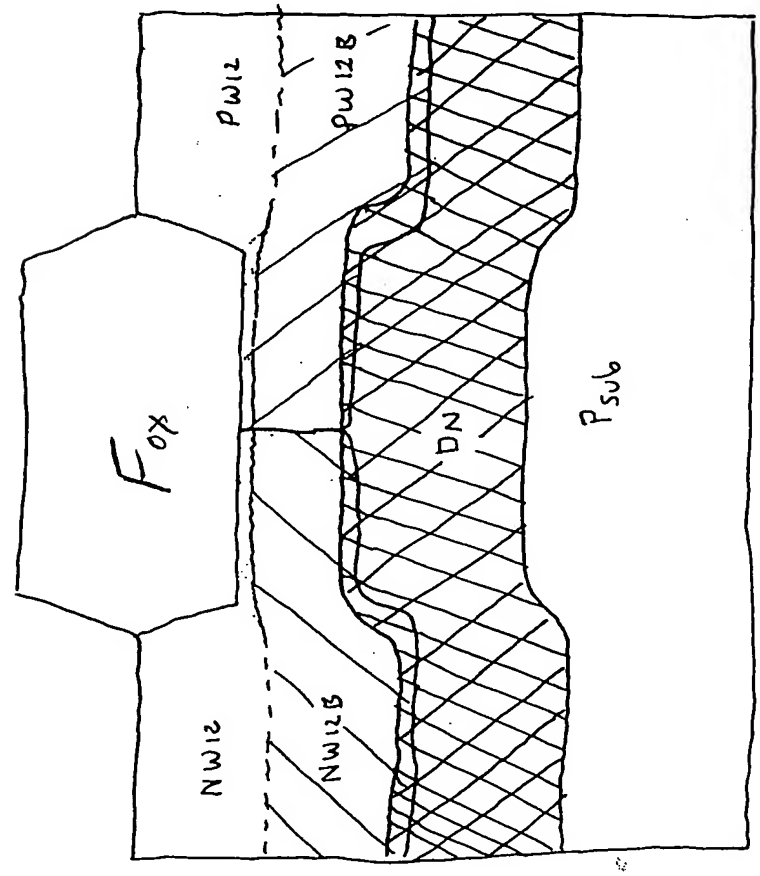


Fig. 15E



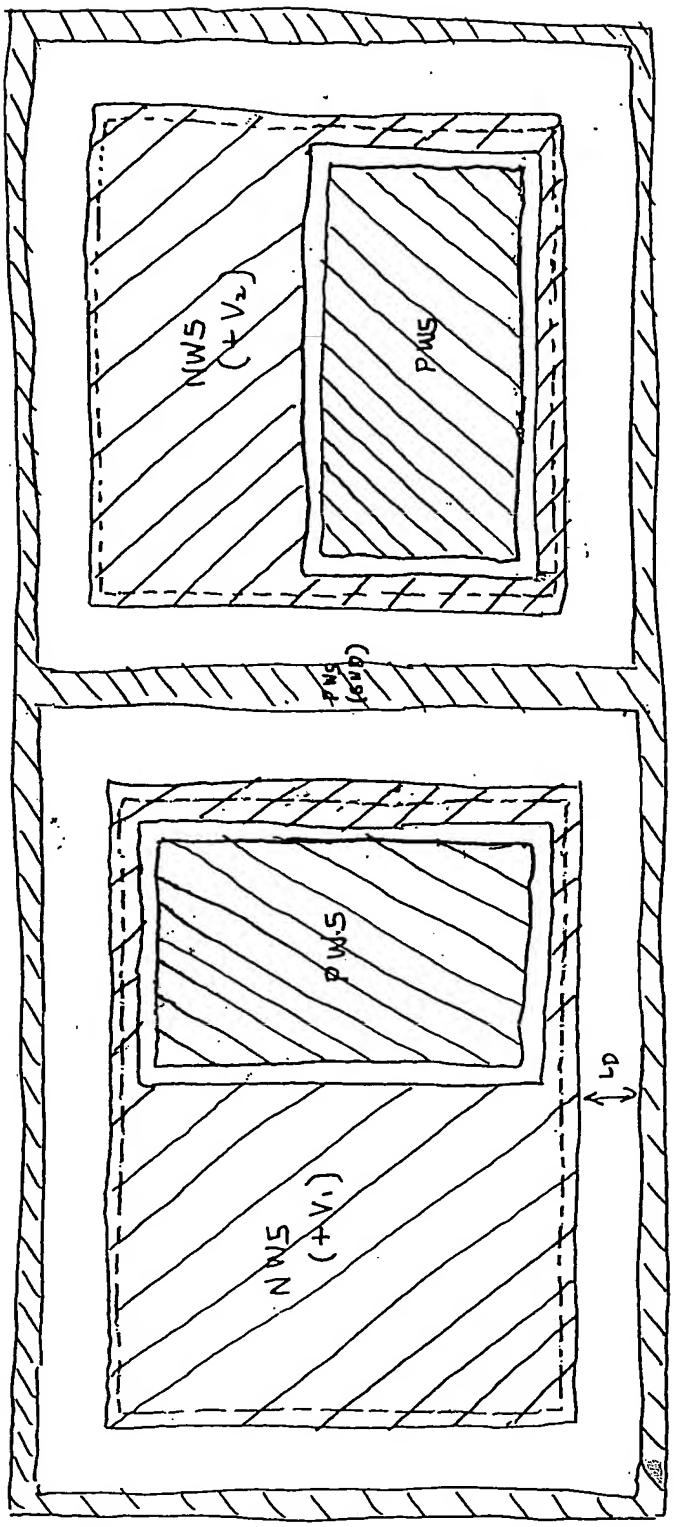
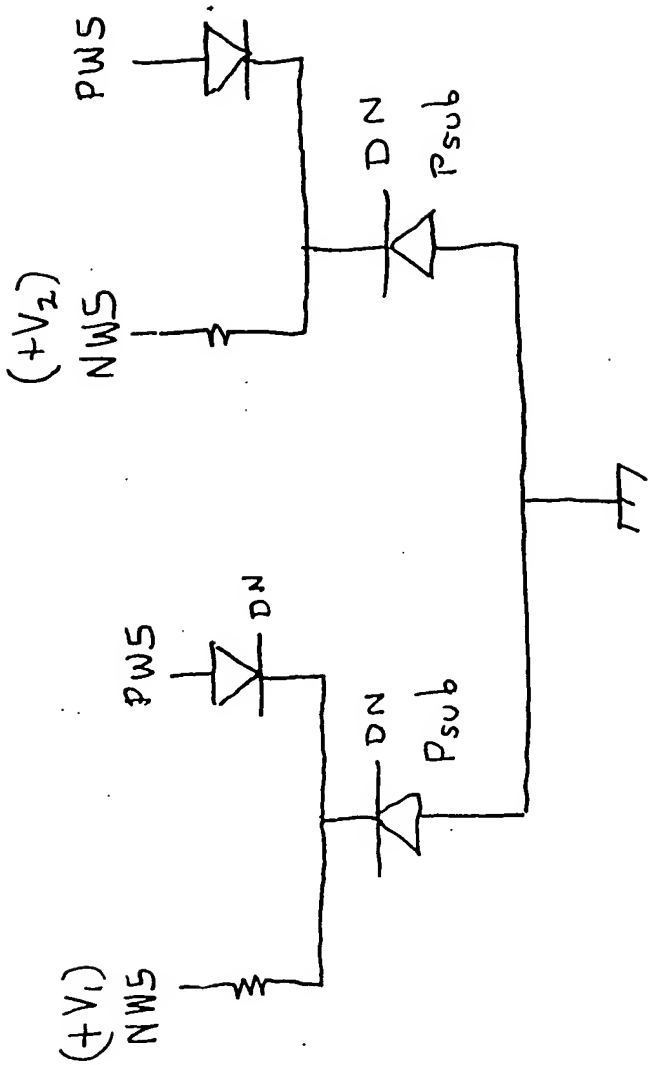


Fig. 16B

Fig. 16C



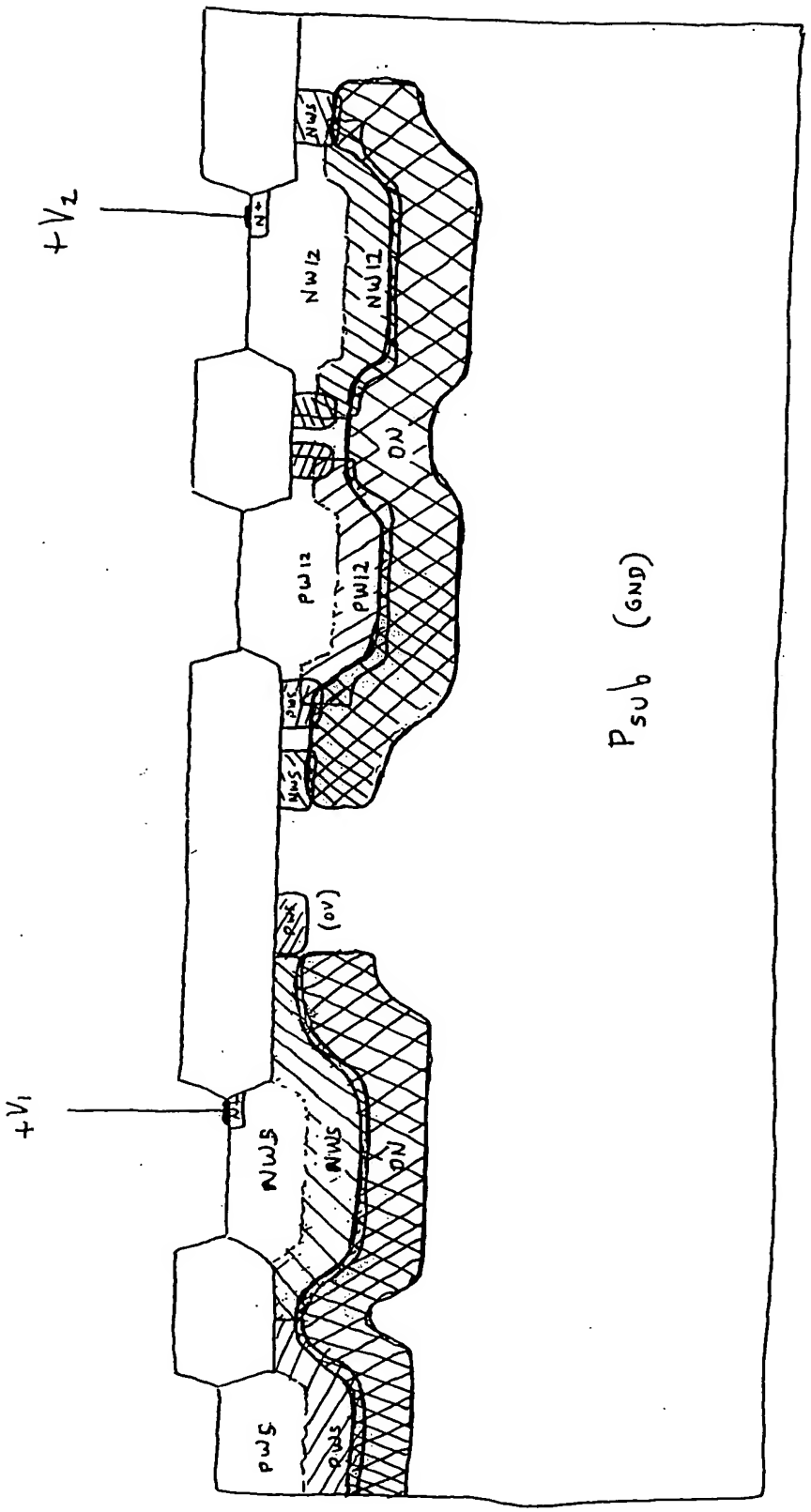
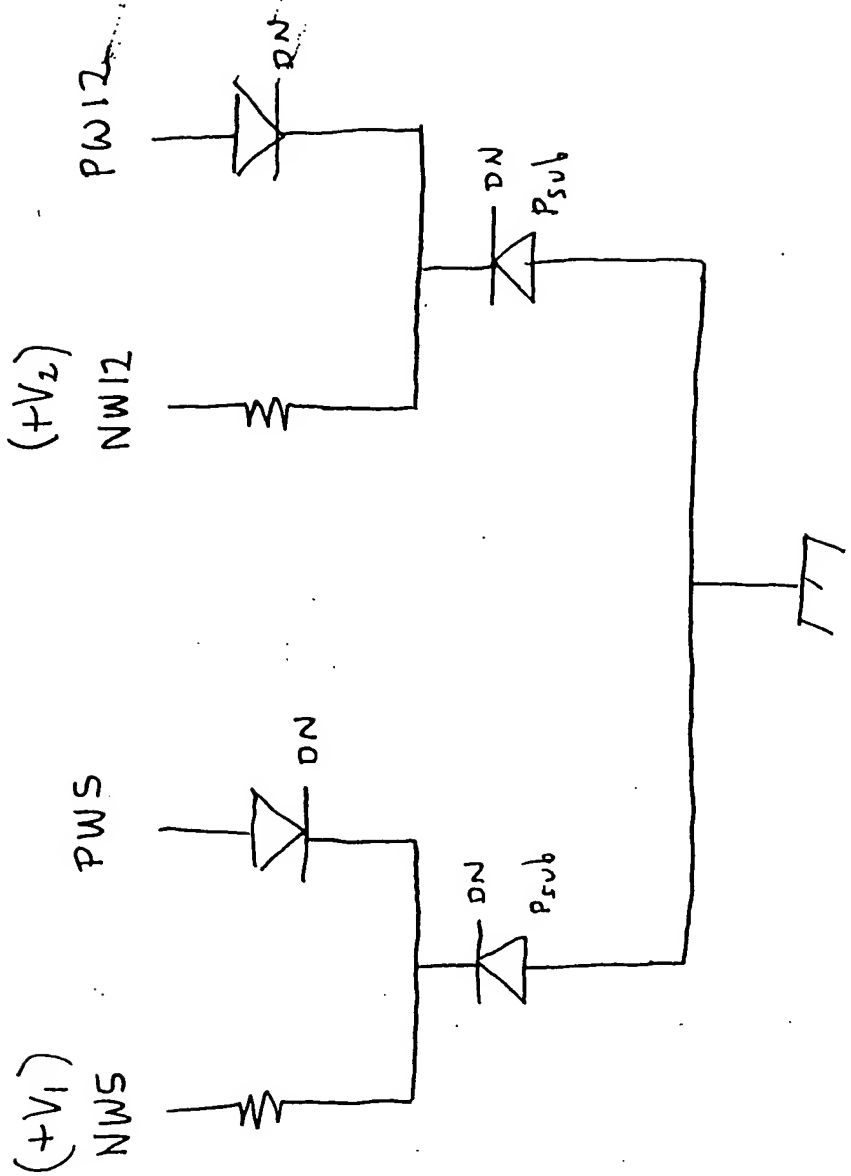


Fig. 16D

Fig. 16E



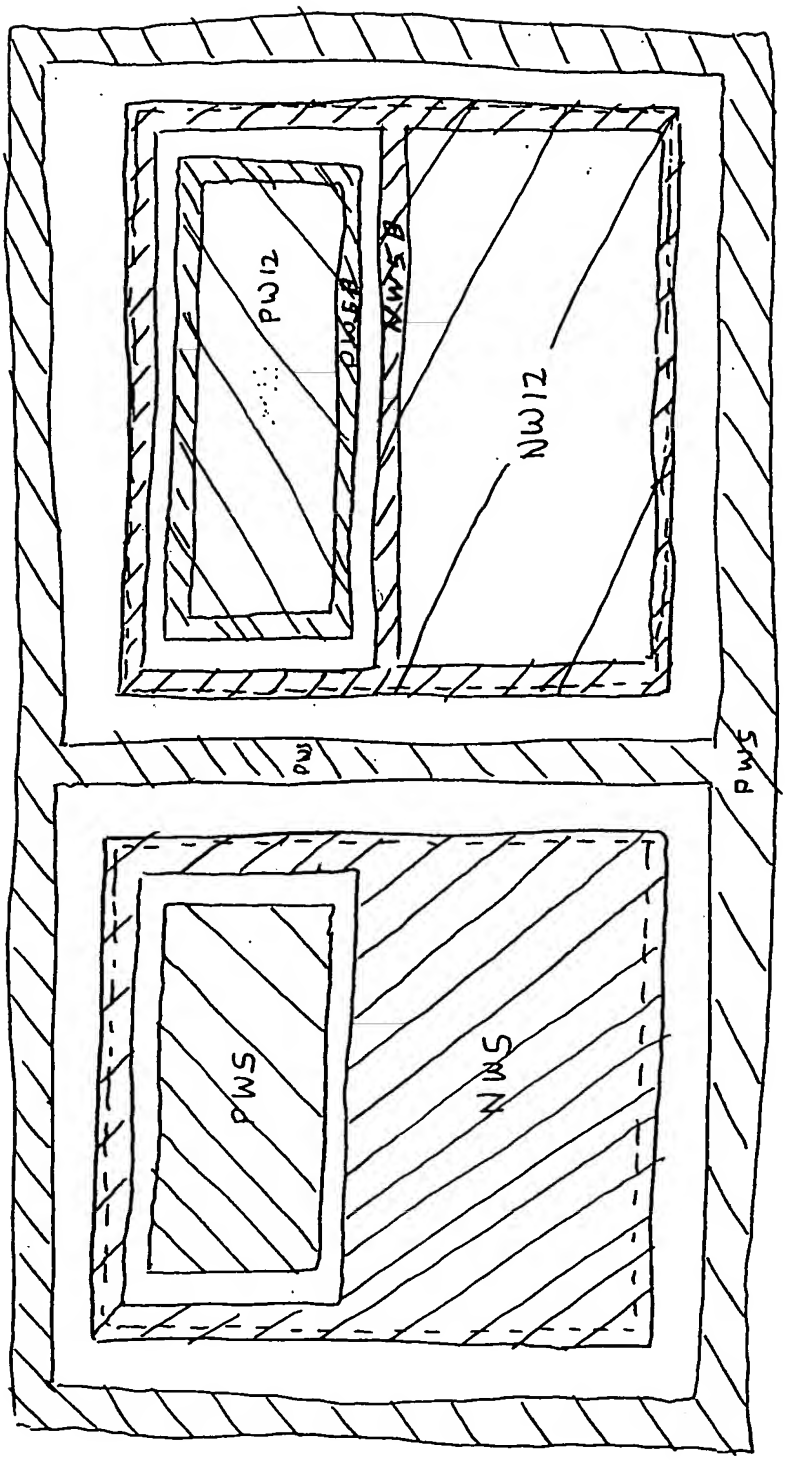


Fig. 16F

Fig. 17A

Prior Art

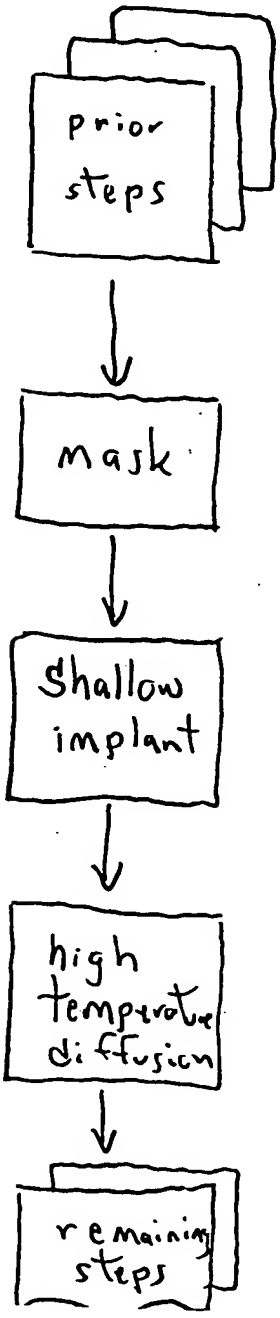


Fig. 17B

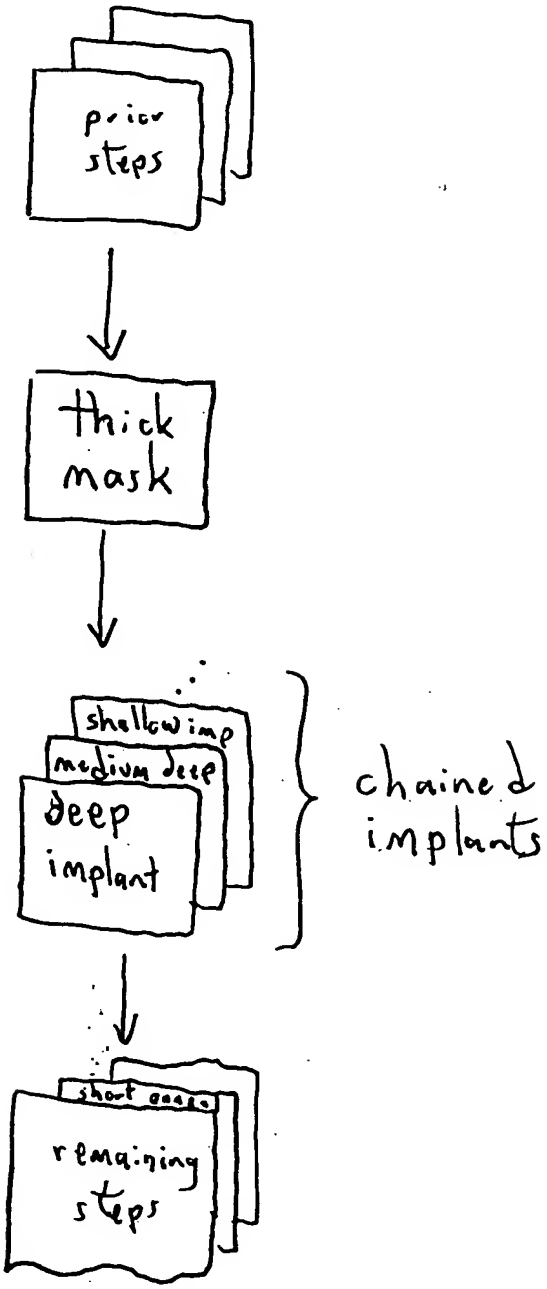


Fig. 17D

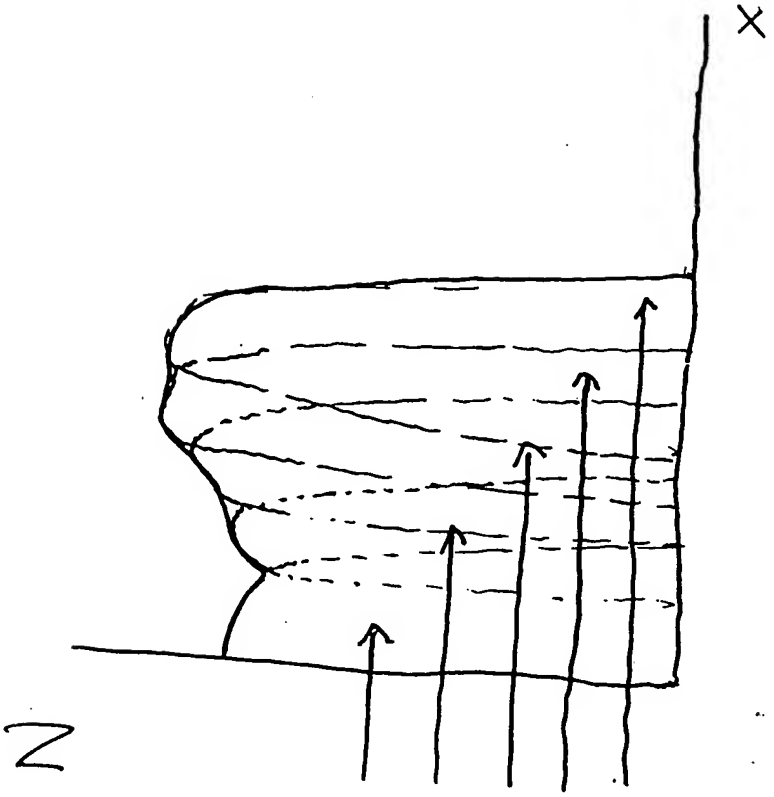


Fig. 17C

Prior Art

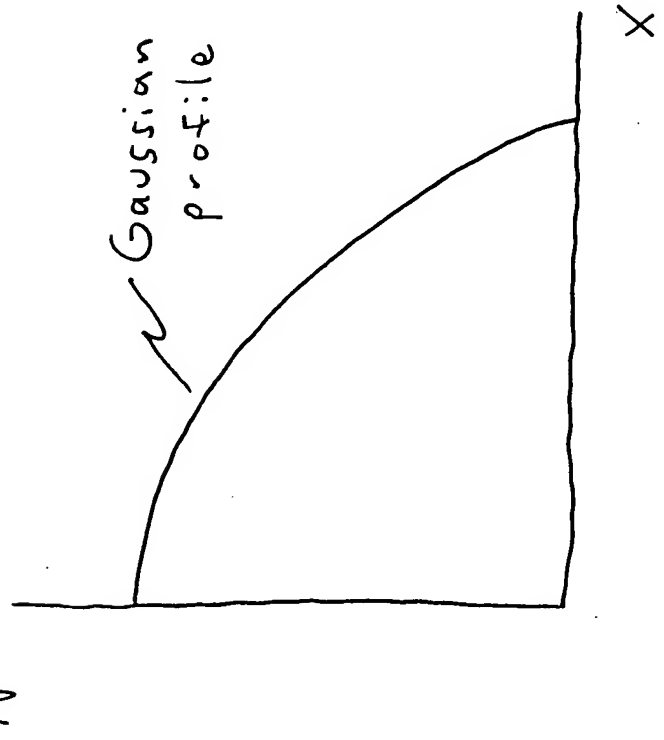


Fig. 17F

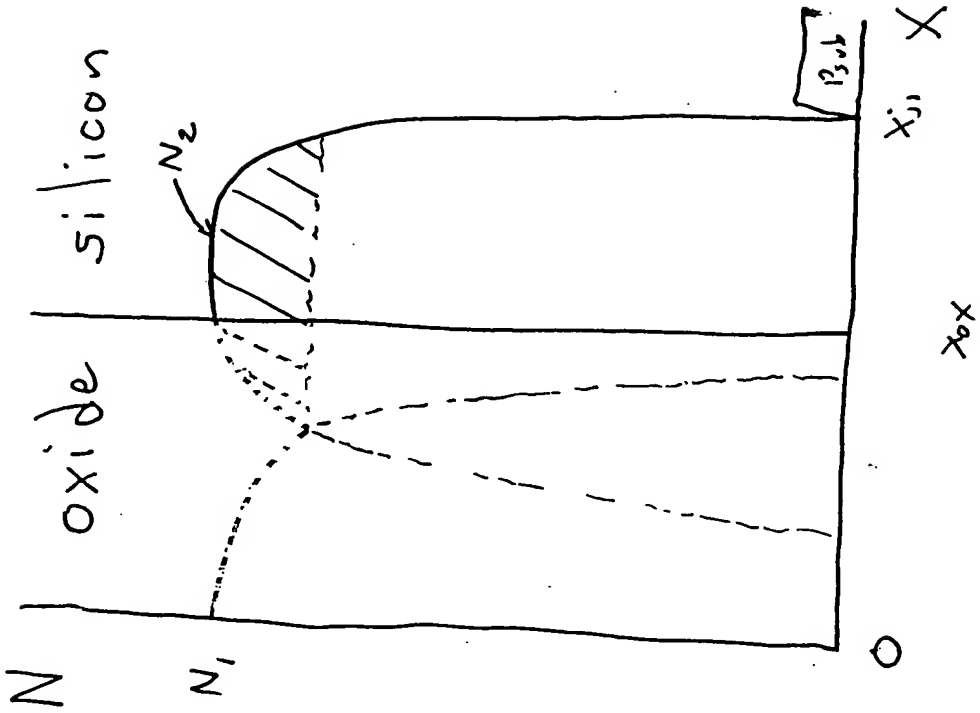
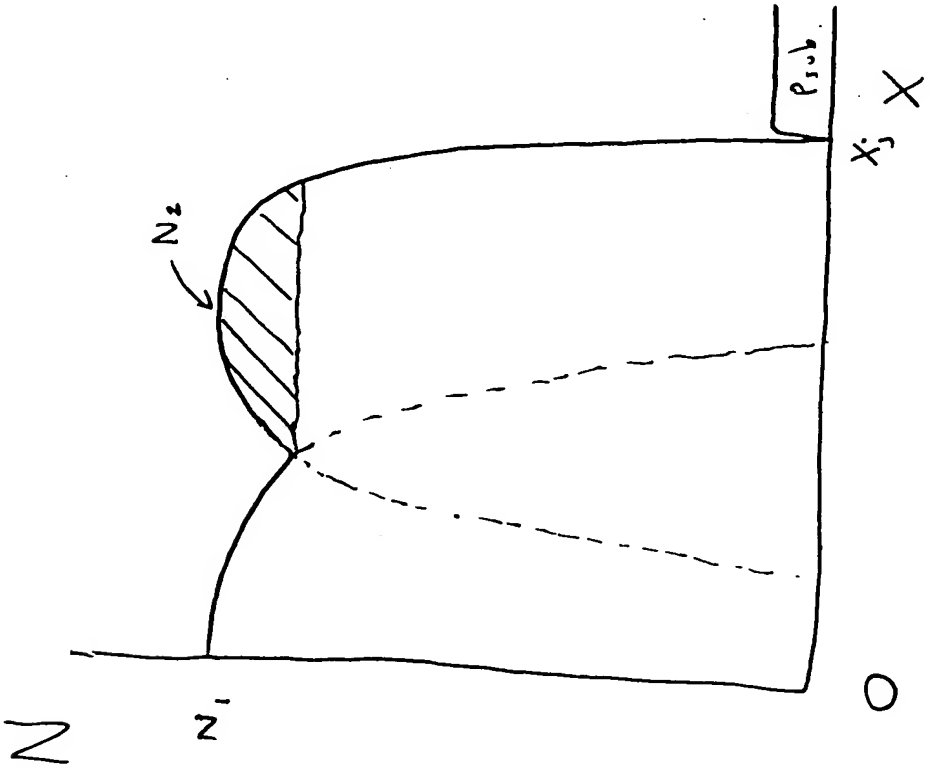


Fig. 17E



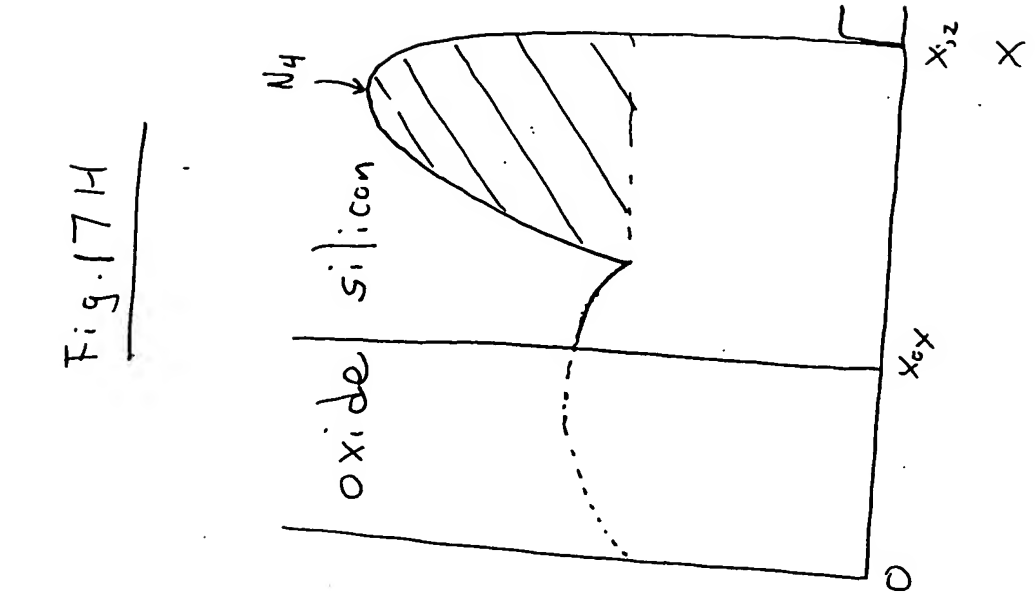


Fig. 17H

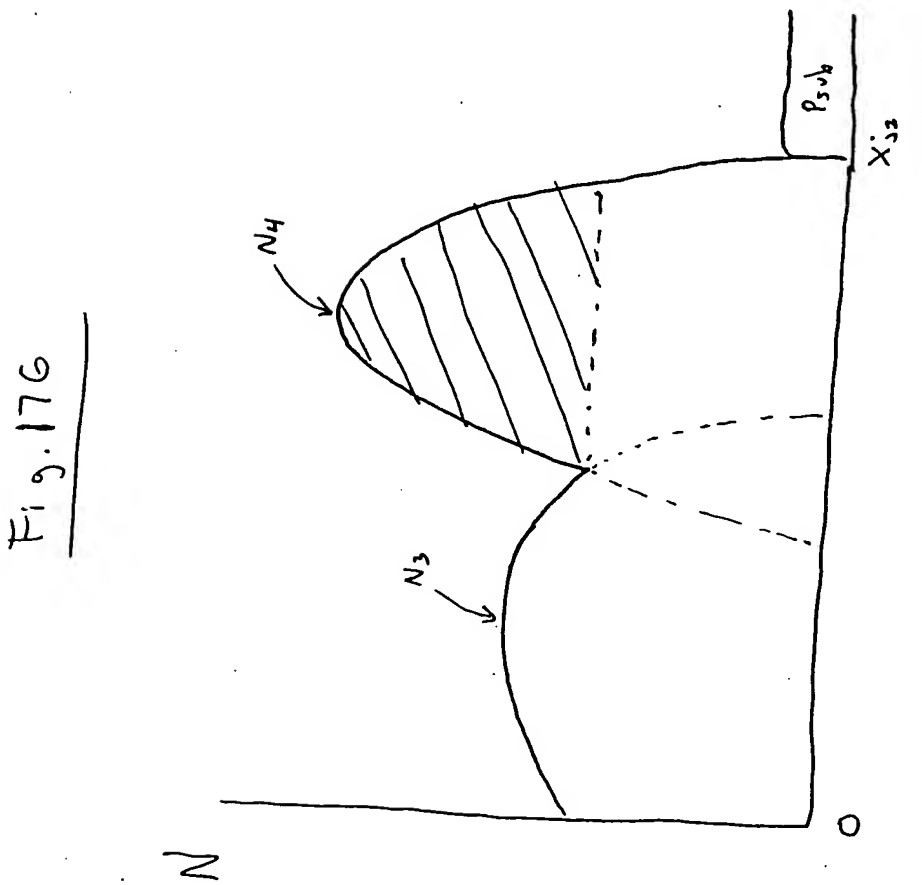


Fig. 17G

Fig. 17J

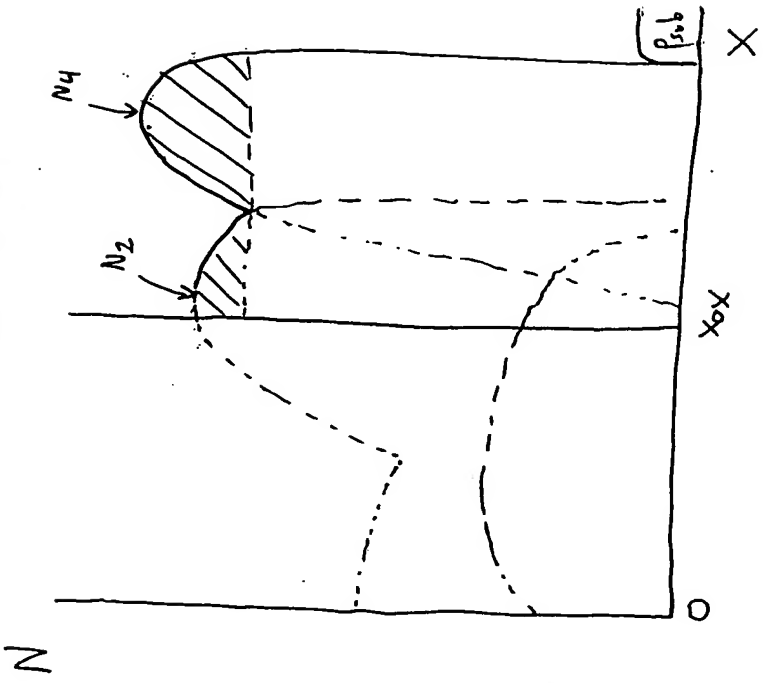
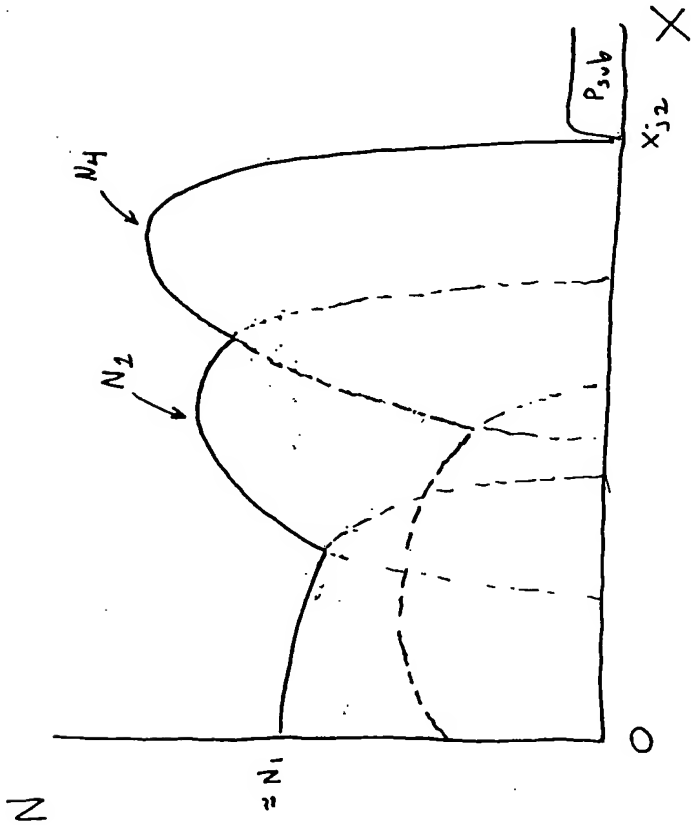


Fig. 17I



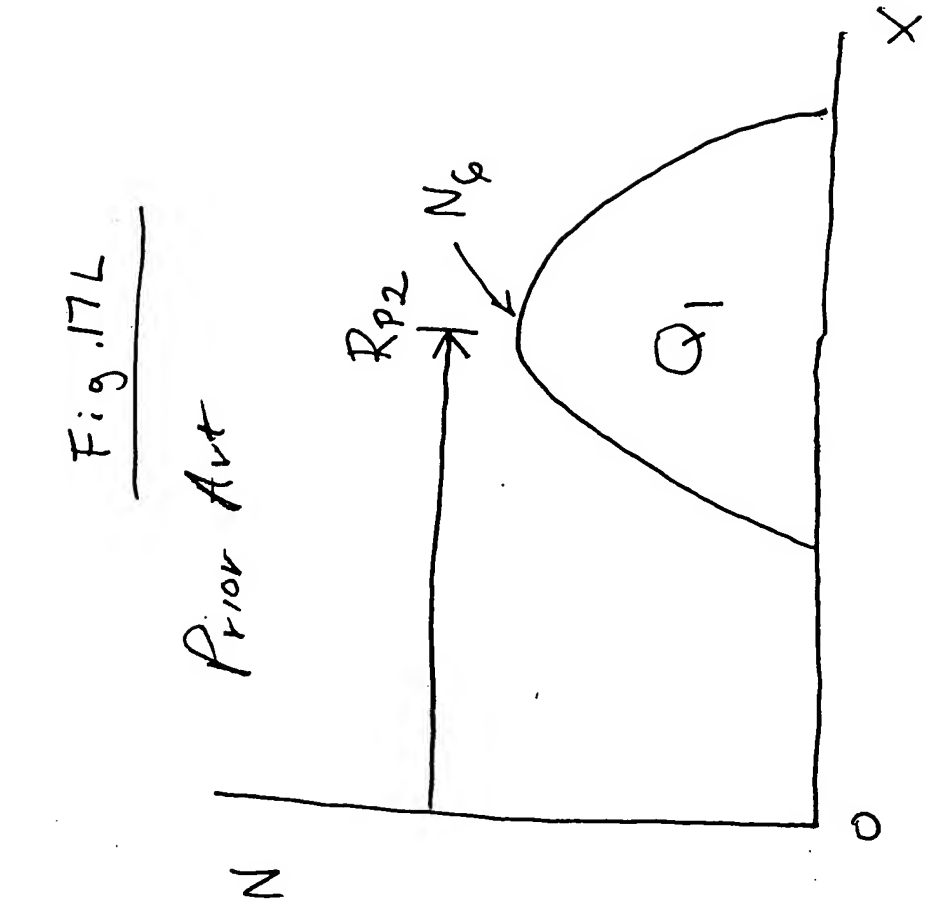


Fig. 17L
Prior Art

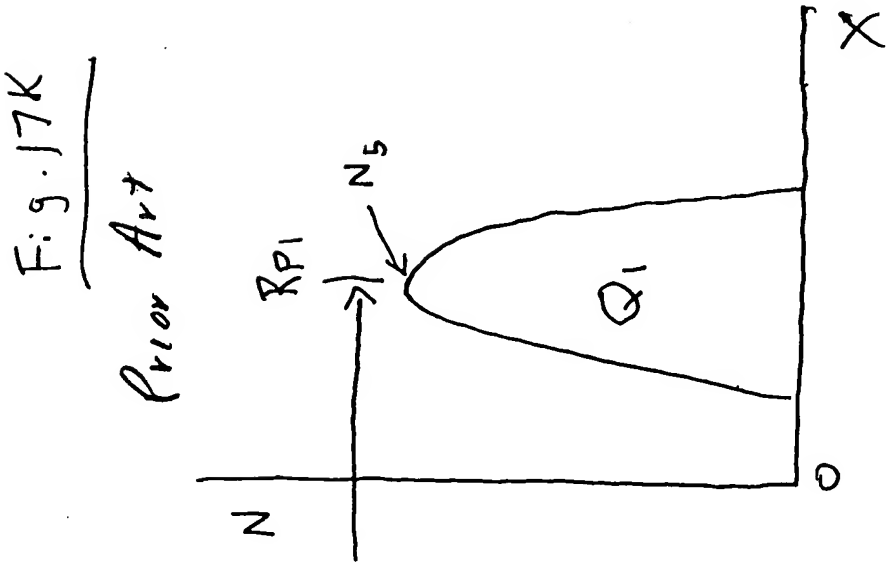


Fig. 17K
Prior Art

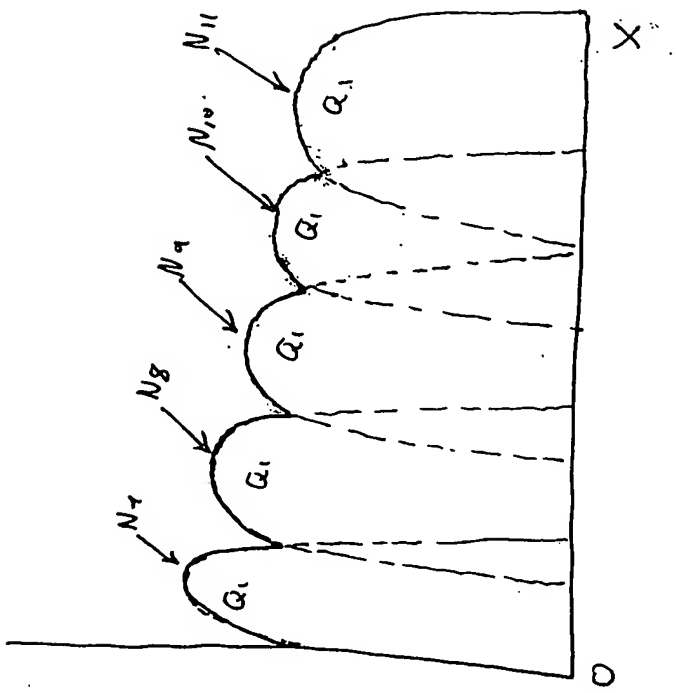


Fig. 17N

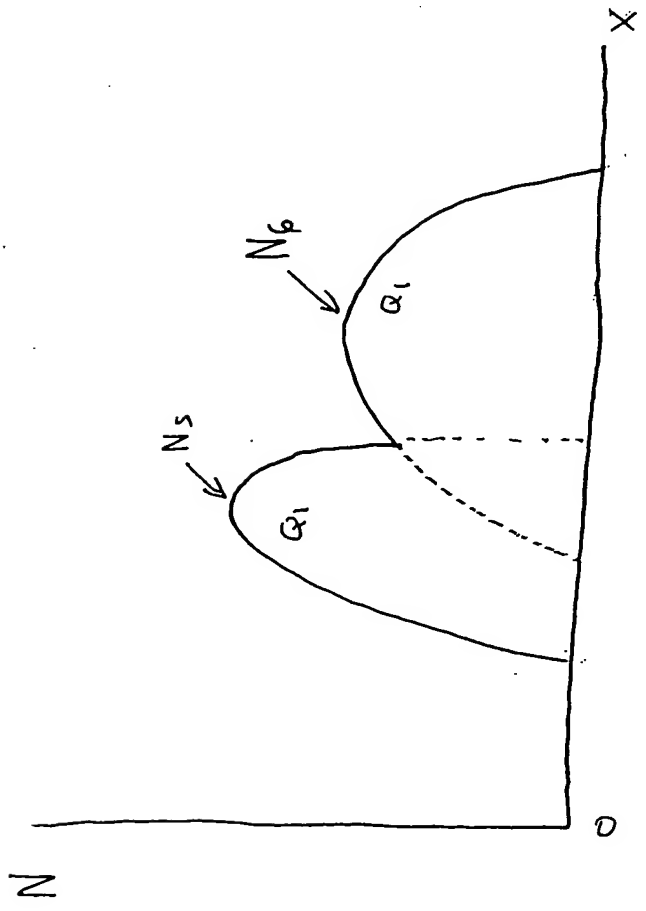


Fig. 17M

Fig. 17Q

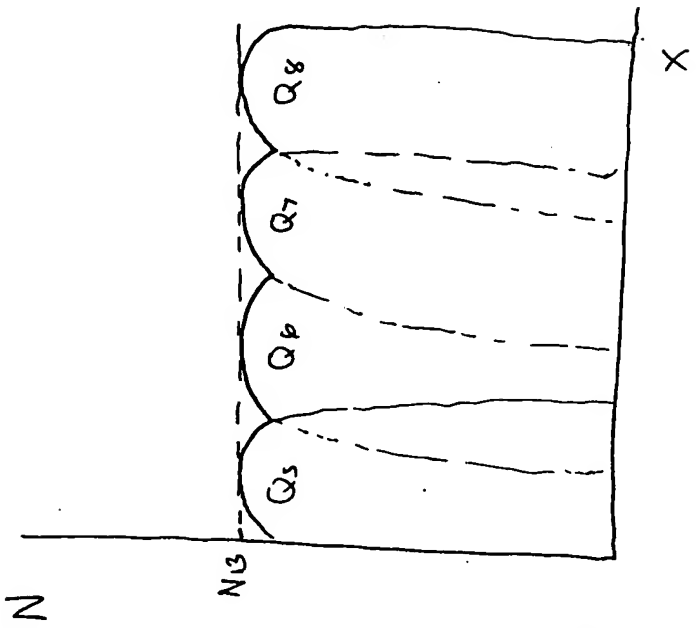


Fig. 17P

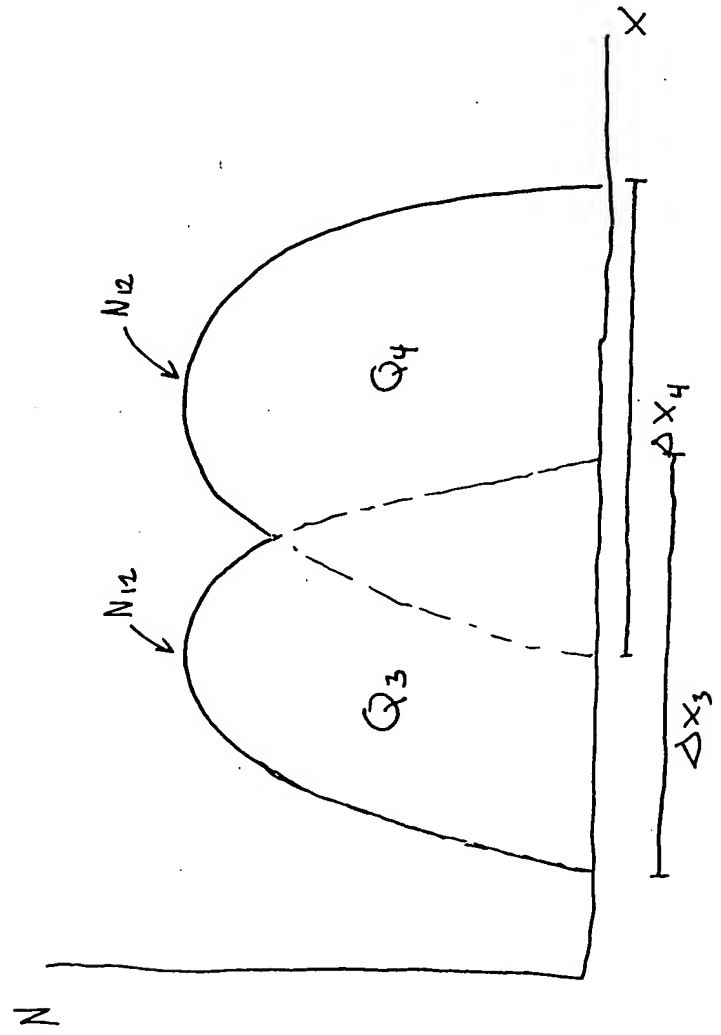


Fig. 17S

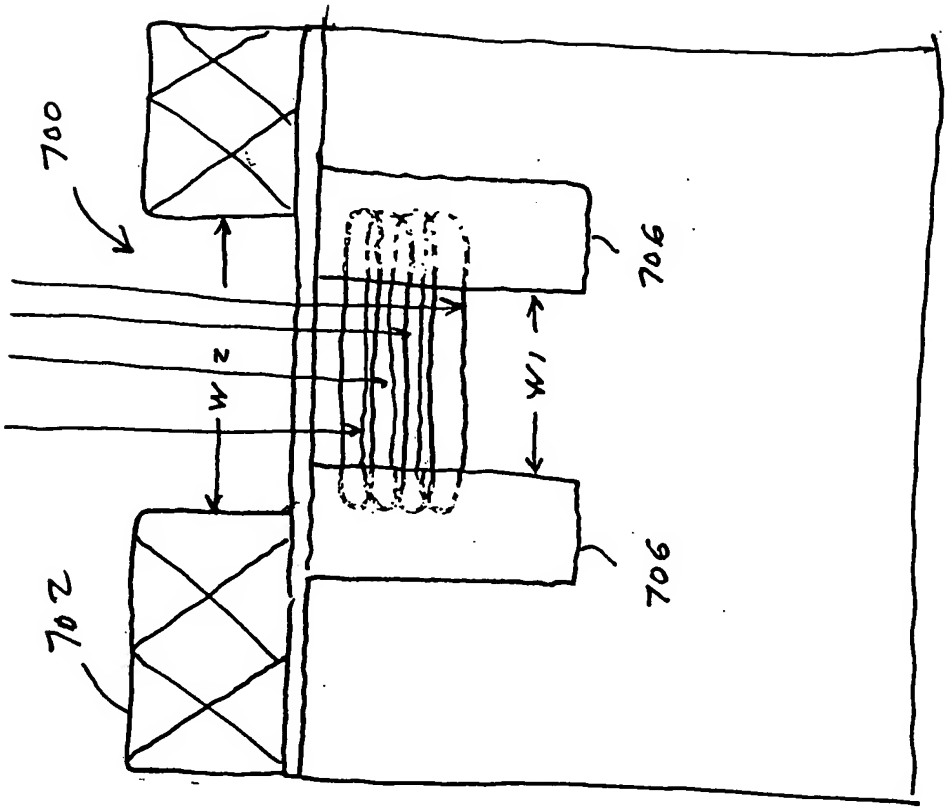


Fig. 17R

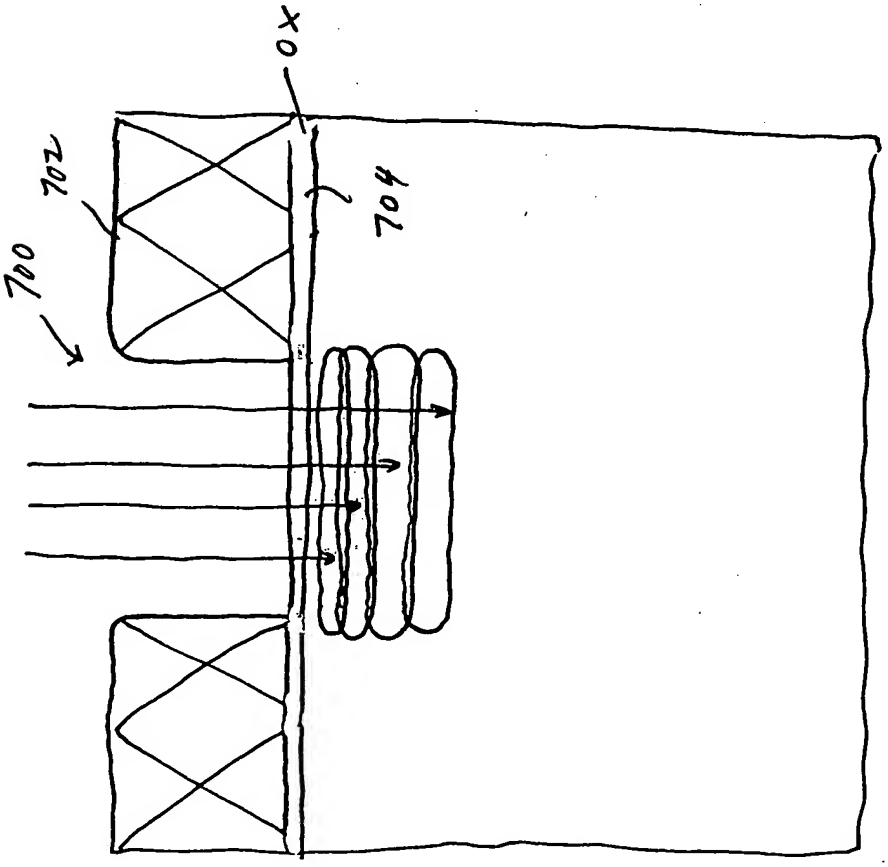


Fig. 17U

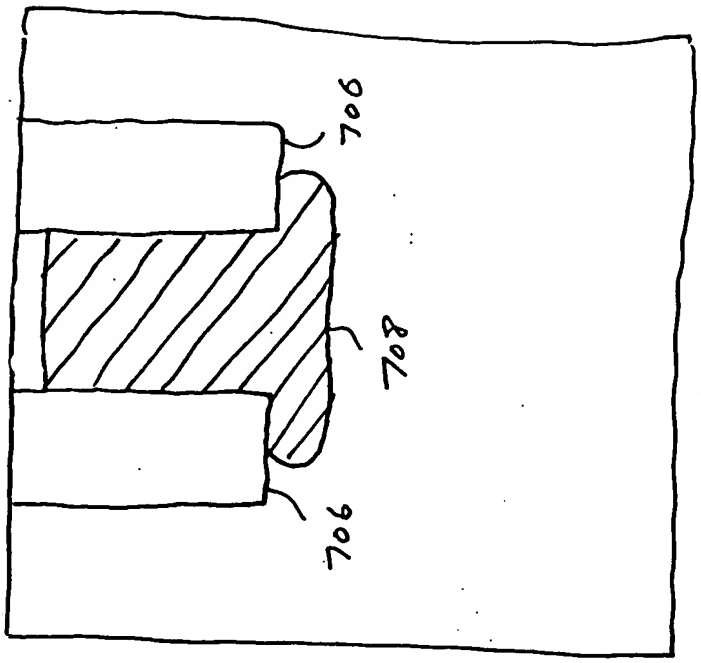
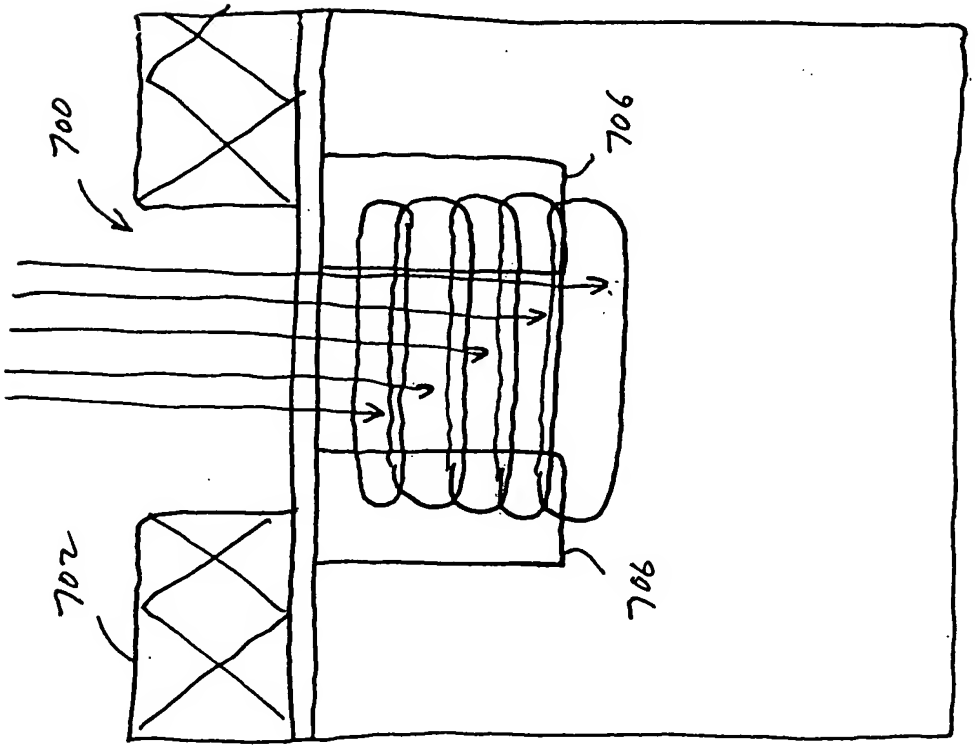


Fig. 17T



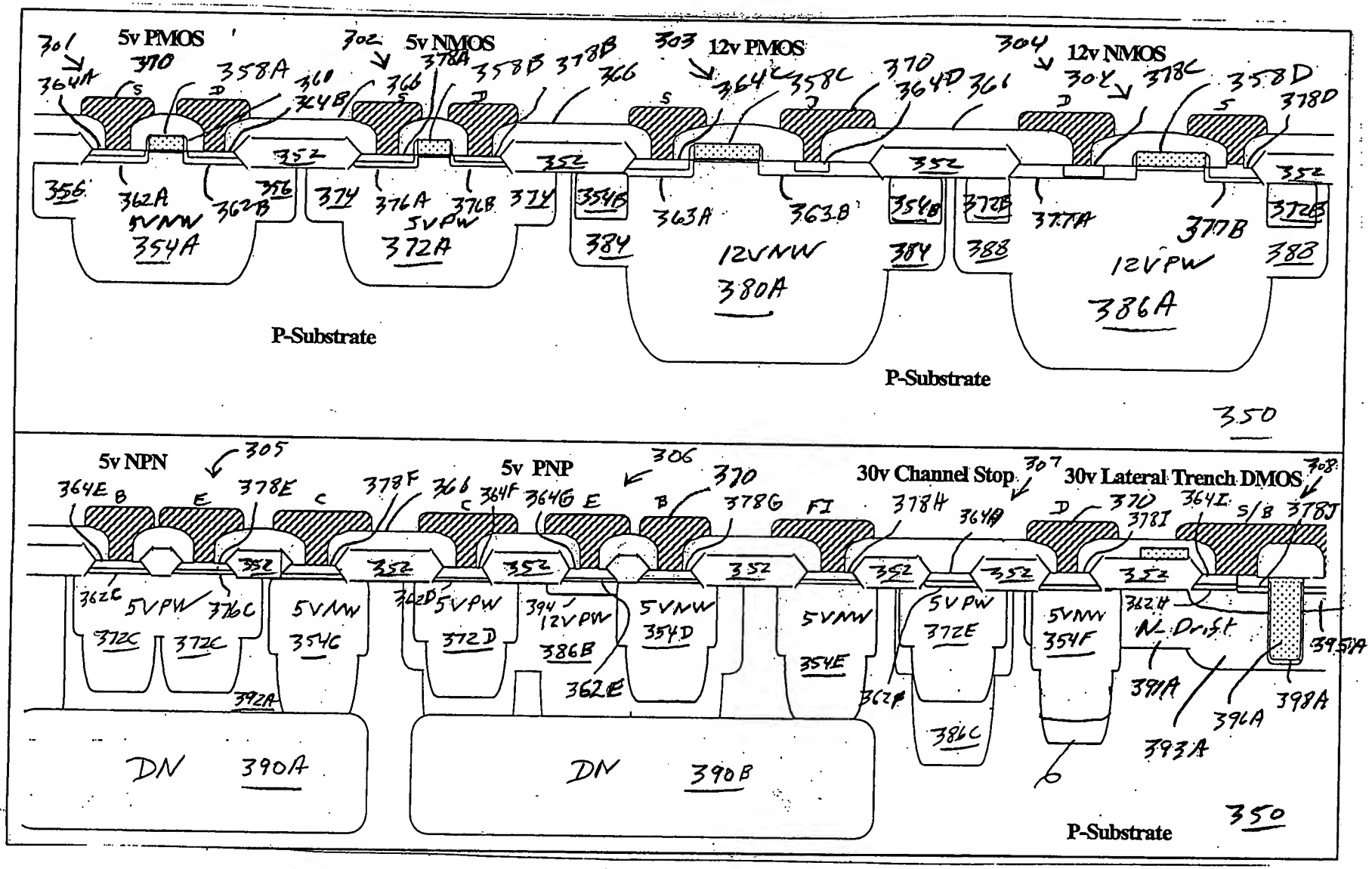

5v PMOS
5v NMOS
12v PMOS
12v NMOS
P-Substrate
5v NPN
5v PNP
30v Channel Stop
30v Lateral Trench DMOS
P-Substrate
DN
DN
P-Substrate

Fig. 18A

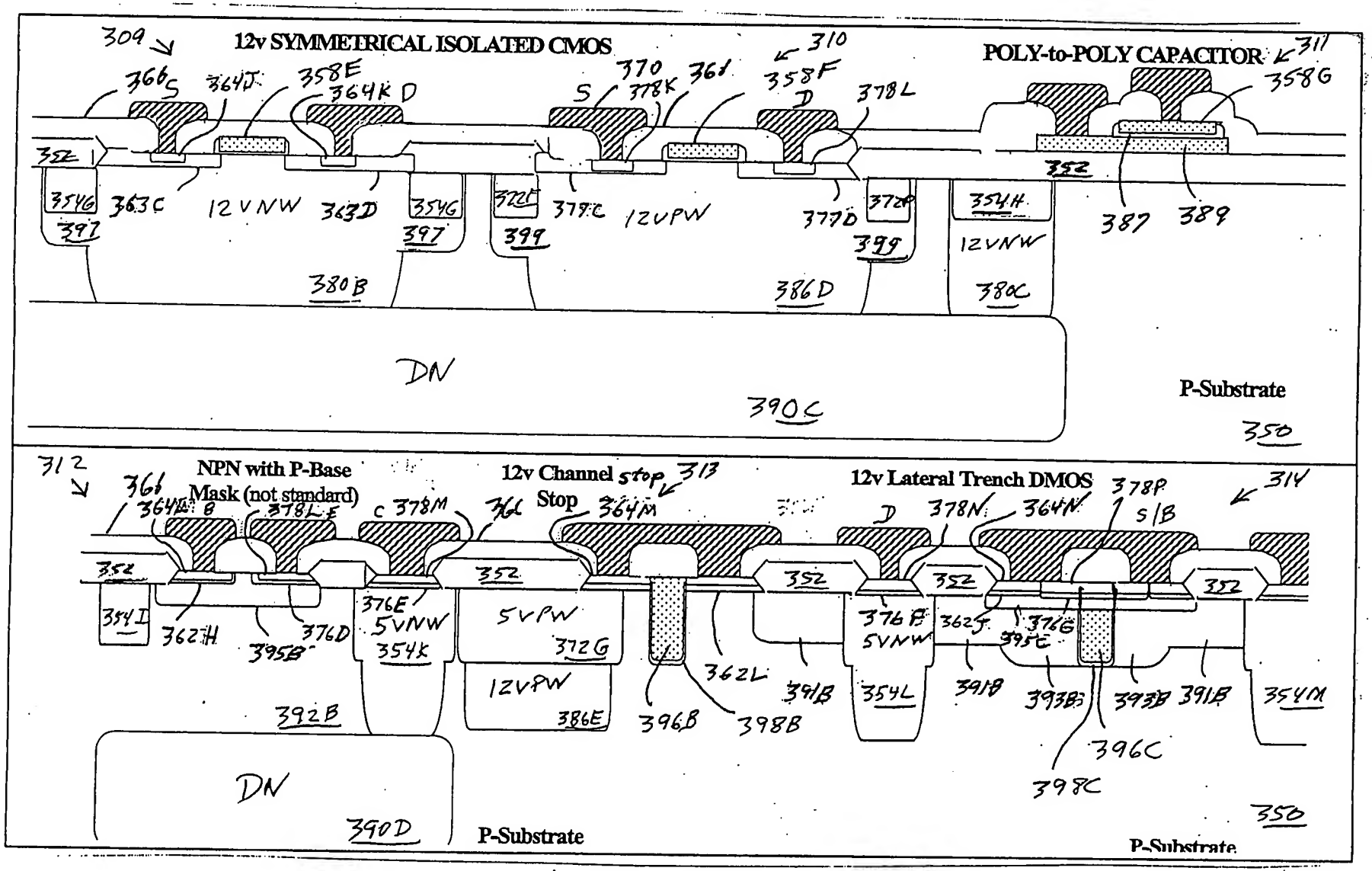


Fig. 18B

77/219

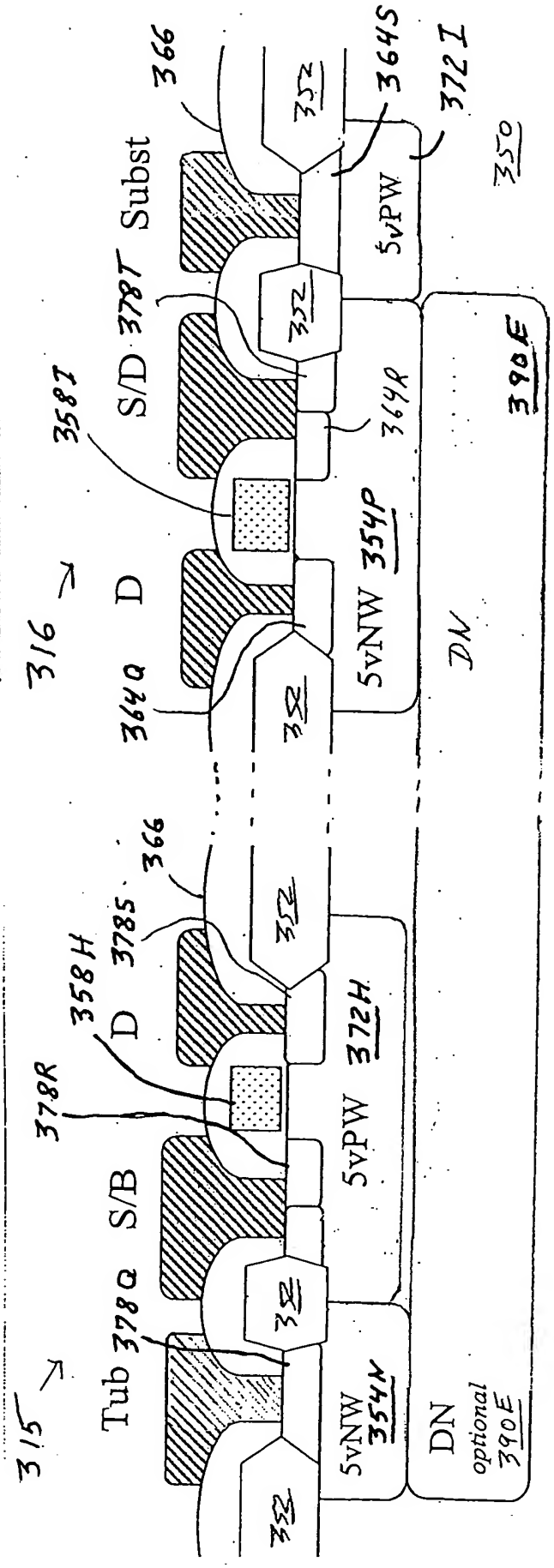

315
316
350
Tub
S/B
D
S/D
Subst
378Q
378R
358H
358I
378S
378T
366
3785
364Q
364P
364S
372H
372I
5vNW 354N
5vPW 372H
5vNW 354P
5vPW
DN optional 390E
DN
390E
352

Fig. 18C

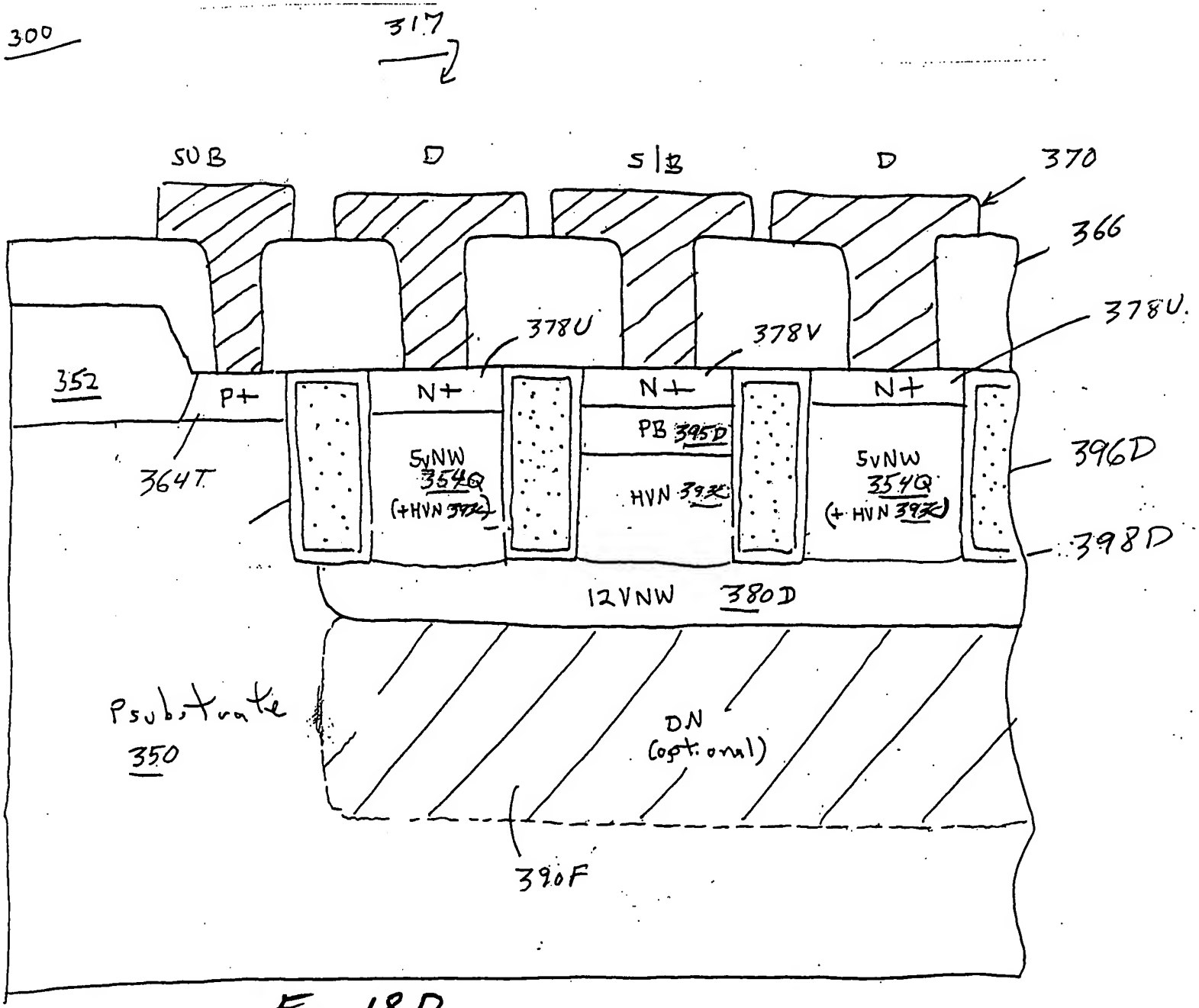

300
317
SUB
D
S/B
D
370
366
378U
378V
378U
352
P+
N+
N+
N+
364T
PB 395D
5VNW
354Q
(+HVN 392)
HVN 392
5VNW
354Q
(+HVN 392)
396D
398D
12VNW 380D
Psubstrate
350
DN
(optional)
390F

Fig. 18D

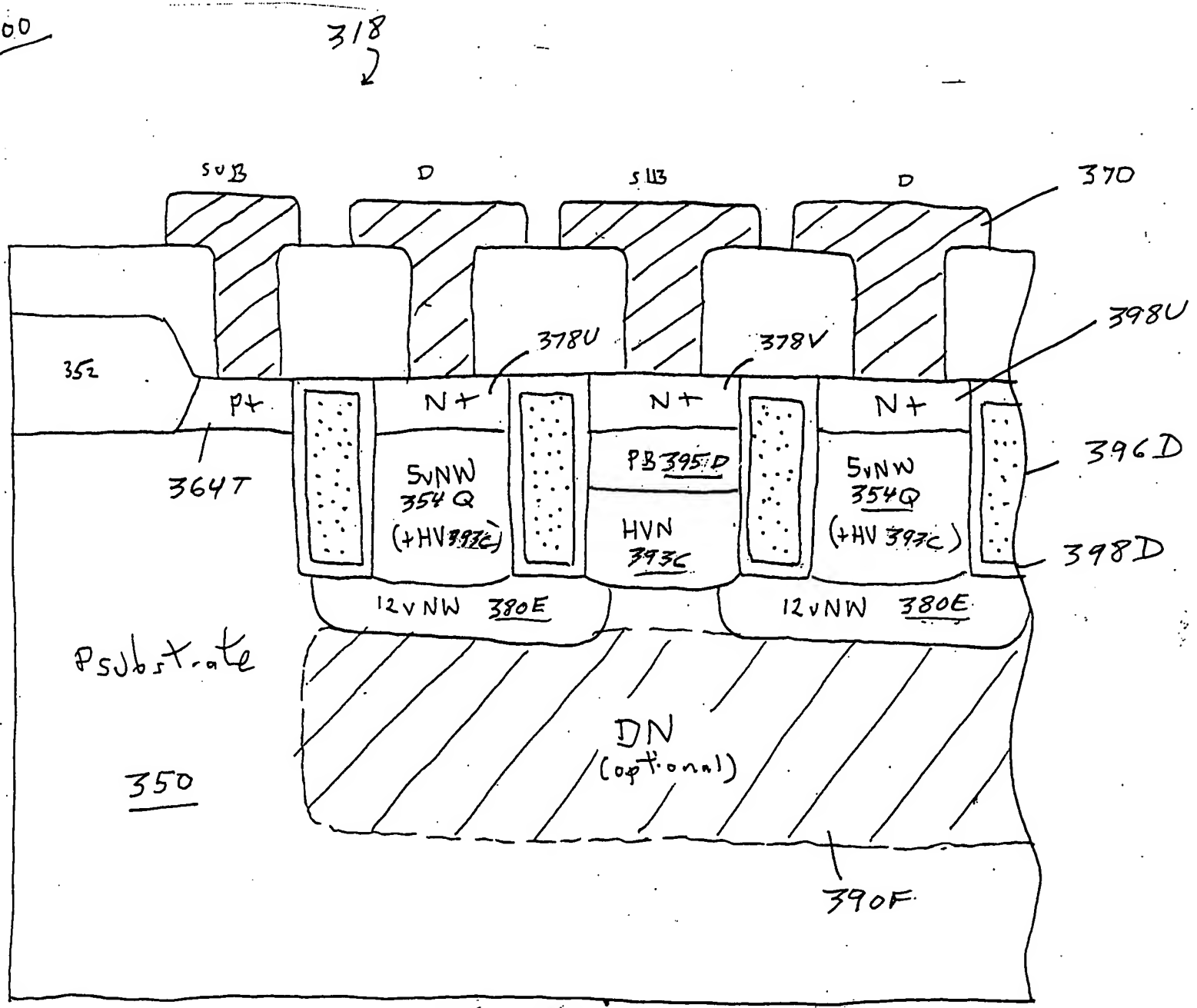

300
318
SUB
D
SUB
D
370
398U
378U
378V
352
P+
N+
N+
N+
364T
5vNW
354Q
(+HV 397C)
PB 395D
HVN
397C
5vNW
354Q
(+HV 397C)
396D
398D
12vNW 380E
12vNW 380E
Psubstrate
DN
(optional)
350
390F

Fig. 18E

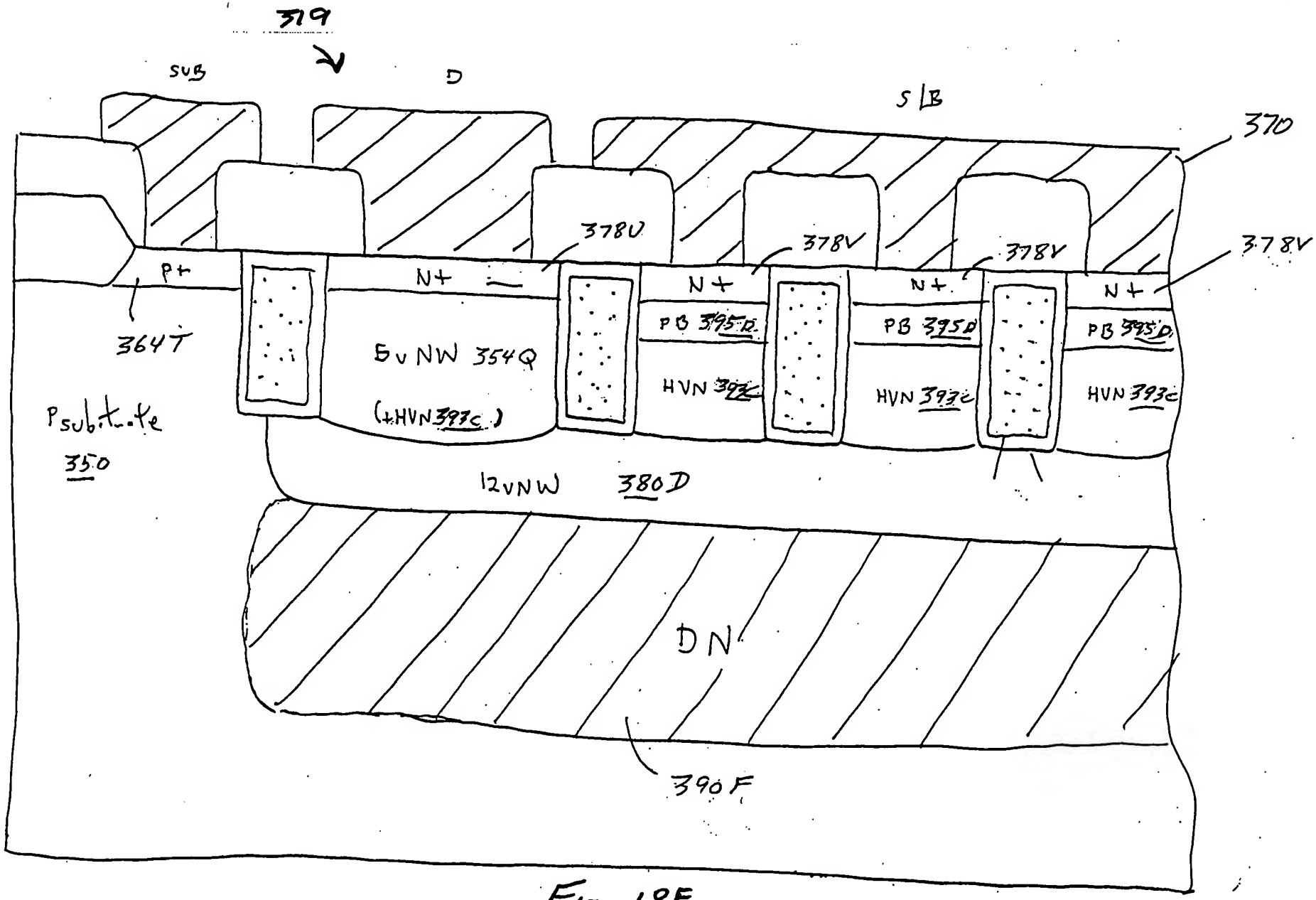

319
SUB
D
SLB
370
378V
378V
378V
378V
P+
N+
N+
N+
N+
364T
PB 395D
PB 395D
PB 395D
5vNW 354Q
(+HVN 393C)
HVN 393C
HVN 393C
HVN 393C
Psubstrate
350
12vNW 380D
DN
390F

Fig. 18F

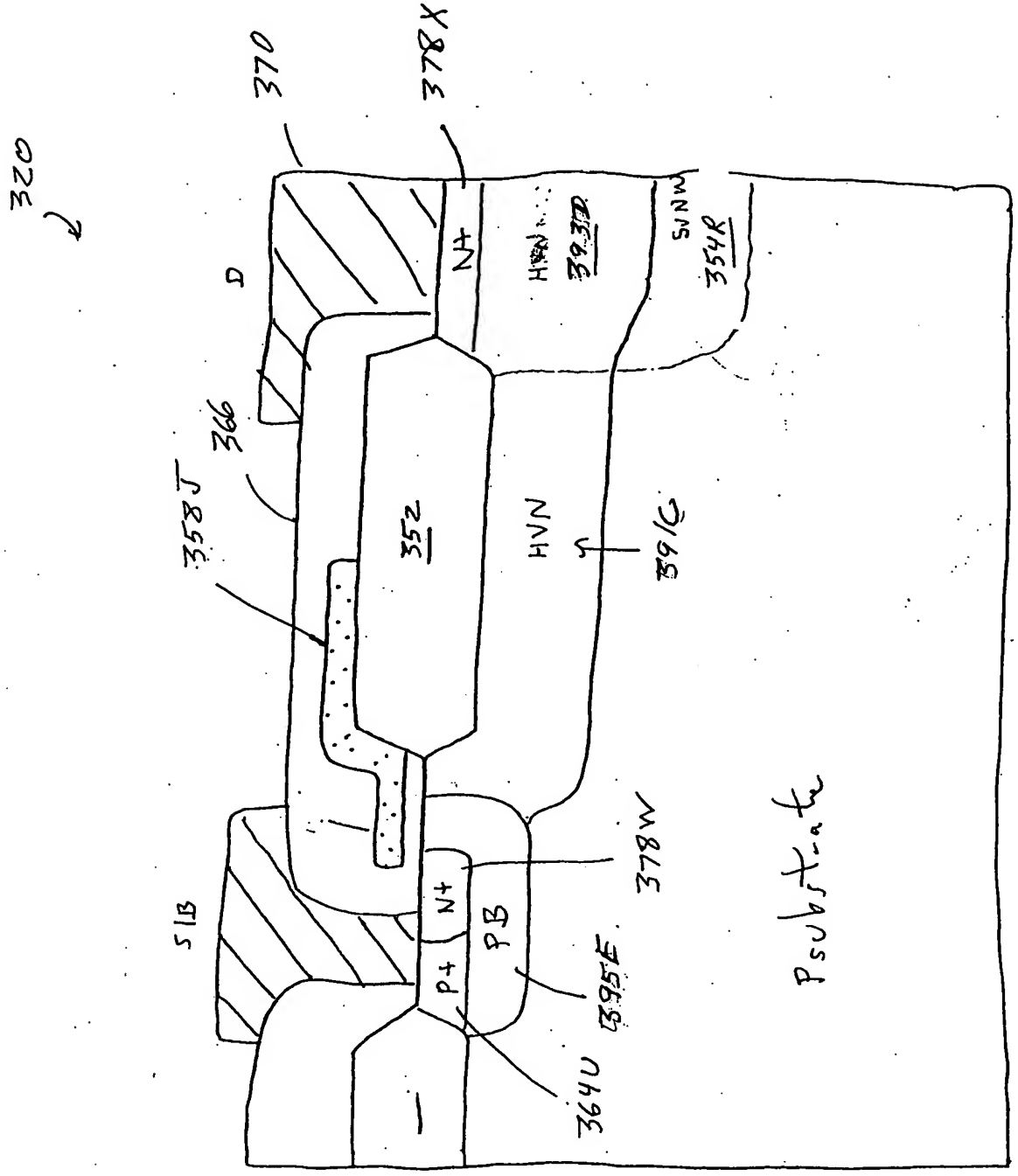

320
370
378X
D
N+
HVN
SiNW
354R
366
358J
352
HVN
391G
SiB
N+
P+
PB
378W
364U
395E
Psubstrate

Fig 18G

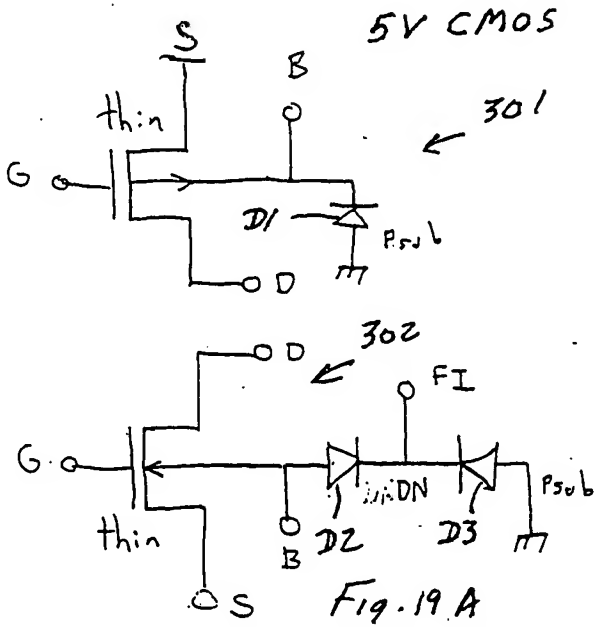


Fig. 19A

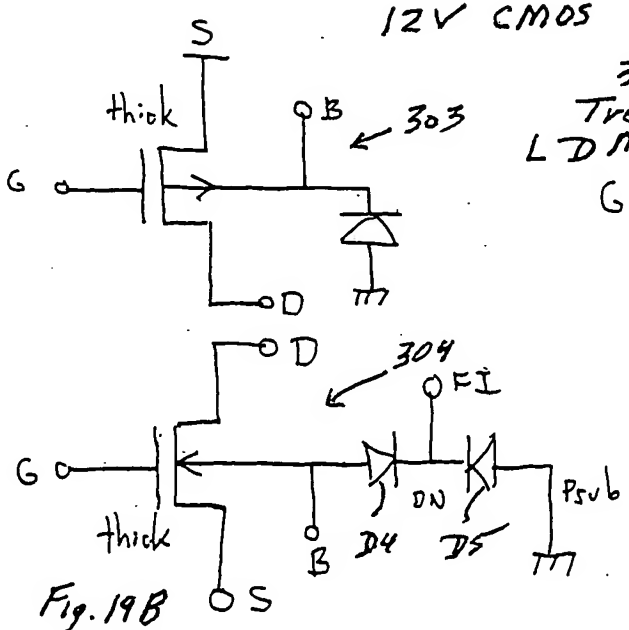


Fig. 19B

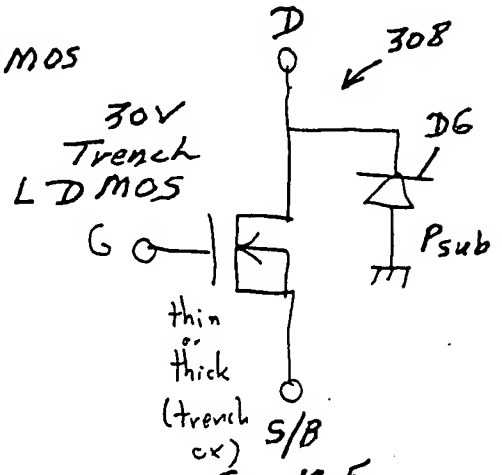


Fig. 19E

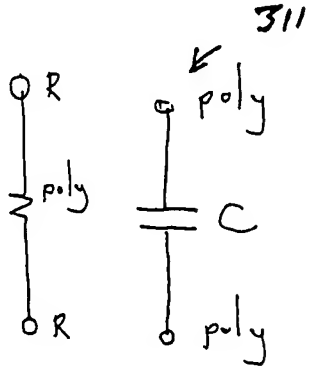


Fig. 19G Fig. 19F

5V NPN

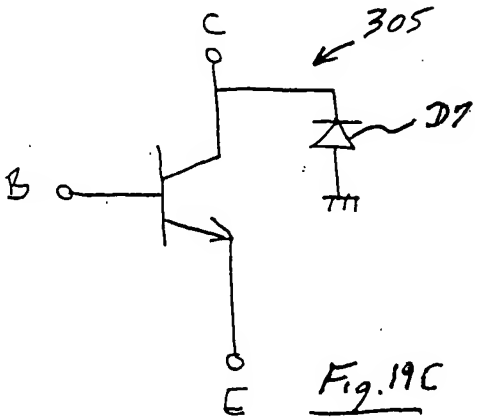


Fig. 19C

5V PNP

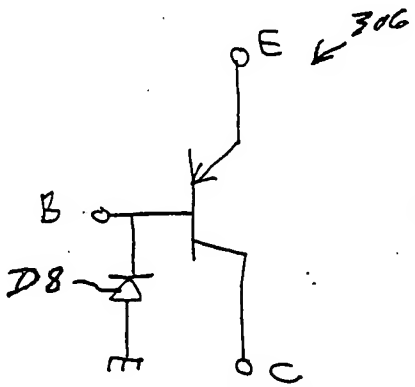


Fig. 19D

30V LDMOS

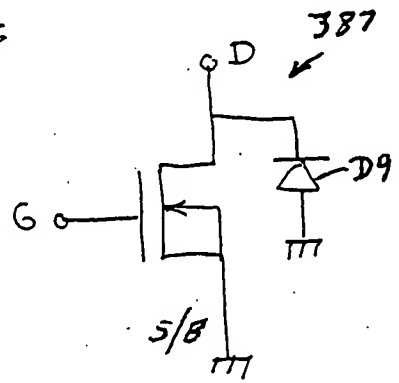
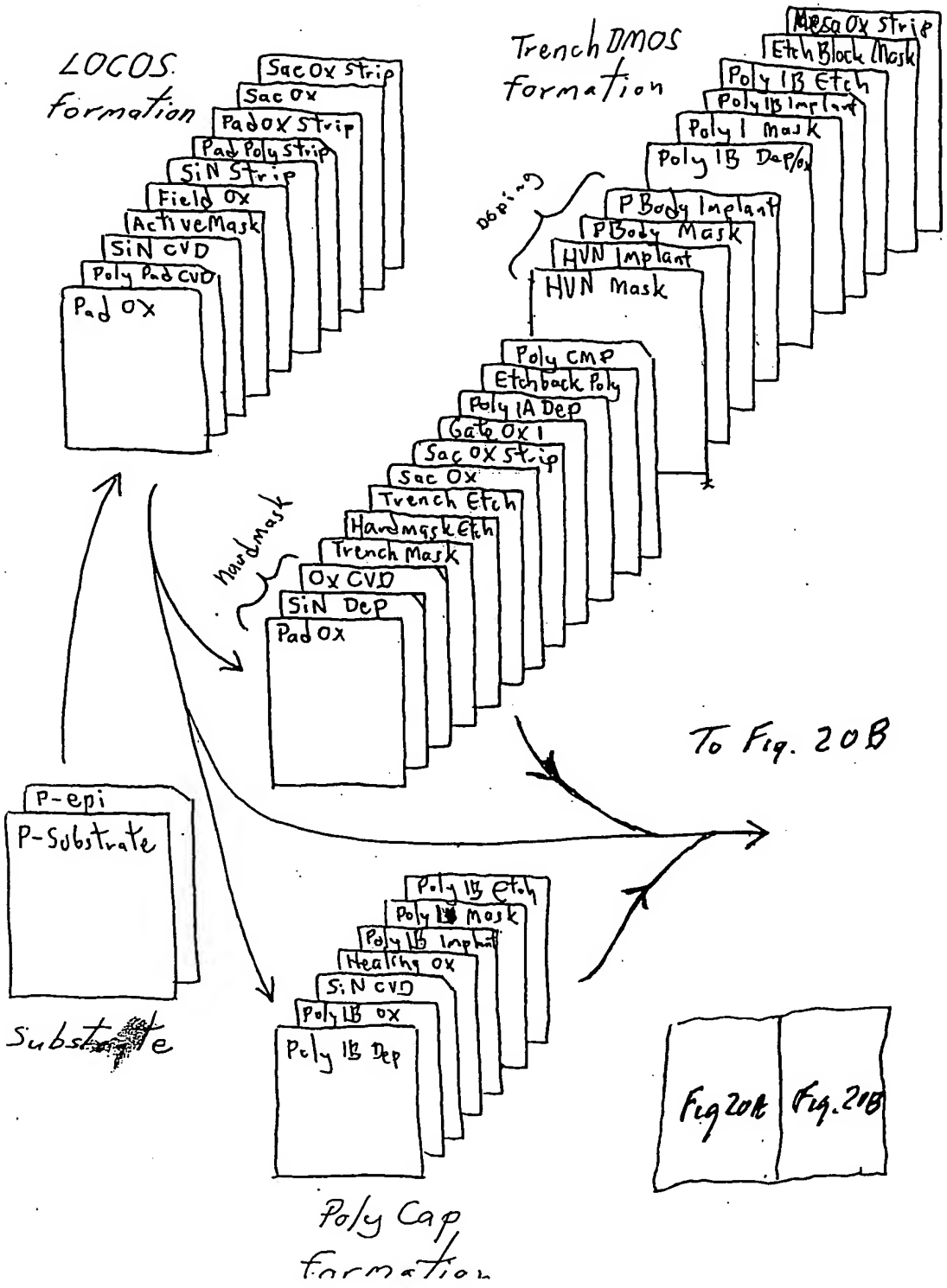


Fig. 19H


LOCOS formation
Sac Ox Strip
Sac Ox
Pad Ox Strip
Pad Poly Strip
SiN Strip
Field Ox
Active Mask
SiN CVD
Poly Pad CVD
Pad Ox
Trench DMOS formation
Mesa Ox Strip
Etch Block Mask
Poly 1B Etch
Poly 1B Implant
Poly 1 Mask
Poly 1B Dep/Ox
Doping
P Body Implant
P Body Mask
HVN Implant
HVN Mask
Poly CMP
Etchback Poly
Poly 1A Dep
Gate Ox 1
Sac Ox Strip
Sac Ox
Trench Etch
Hardmask Etch
Trench Mask
Ox CVD
SiN Dep
Pad Ox
Hardmask
To Fig. 20B
P-epi
P-Substrate
Substrate
Poly 1B Etch
Poly 1B Mask
Poly 1B Implant
Healing Ox
SiN CVD
Poly 1B Ox
Poly 1B Dep
Poly Cap formation
Fig 20A
Fig 20A
Fig. 20B

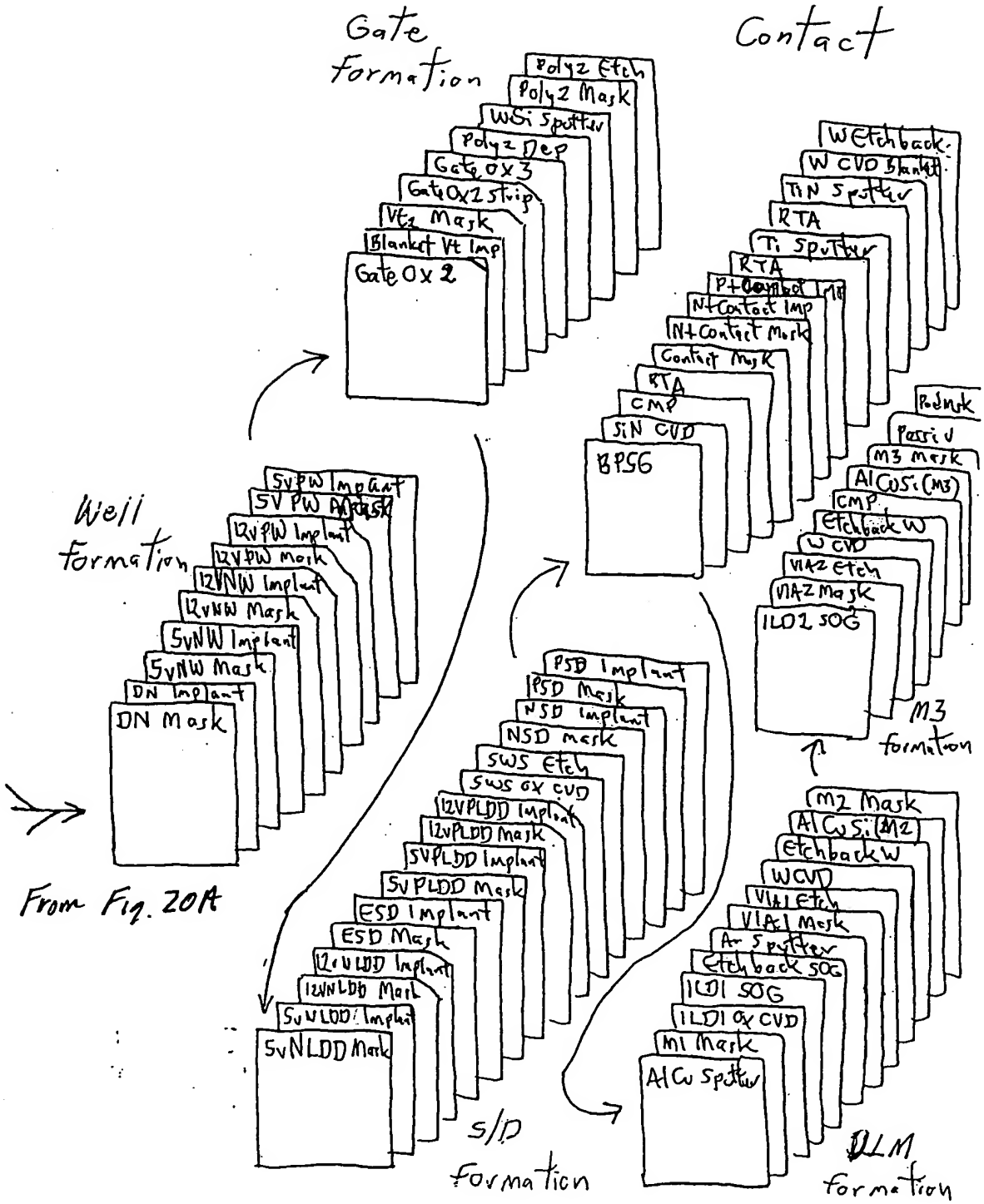

Gate formation
Contact
Well formation
From Fig. 20A
S/D formation
M3 formation
Gate Ox 2
Blanket Vt Imp
Vt2 Mask
Gate Ox2 Strip
Gate Ox3
Poly2 Dep
WSi Sputter
Poly2 Mask
Poly2 Etch
BPSG
SiN CVD
CMP
RTA
Contact Mask
N+Contact Mask
N+Contact Imp
P+Contact Imp
RTA
Ti Sputter
RTA
TiN Sputter
W CVD Blanket
W Etchback
ILD2 SOG
VIA2 Mask
VIA2 Etch
W CVD
Etchback W
CMP
AlCuSi (M3)
M3 Mask
Passiv
Pad Mask
DN Mask
DN Implant
5VNW Mask
5VNW Implant
12VNW Mask
12VNW Implant
12VPW Mask
12VPW Implant
5VPW Mask
5VPW Implant
5VNLDD Mask
5VNLDD Implant
12VNLDD Mask
12VNLDD Implant
ESD Mask
ESD Implant
5VPLDD Mask
5VPLDD Implant
12VPLDD Mask
12VPLDD Implant
SWS ox CVD
SWS Etch
NSD mask
NSD Implant
PSD Mask
PSD Implant
AlCu Sputter
M1 Mask
ILD1 ox CVD
ILD1 SOG
Etchback SOG
Ar Sputter
VIA1 Mask
VIA1 Etch
W CVD
Etchback W
AlCuSi (M2)
M2 Mask
M1M formation

Fig. 20B

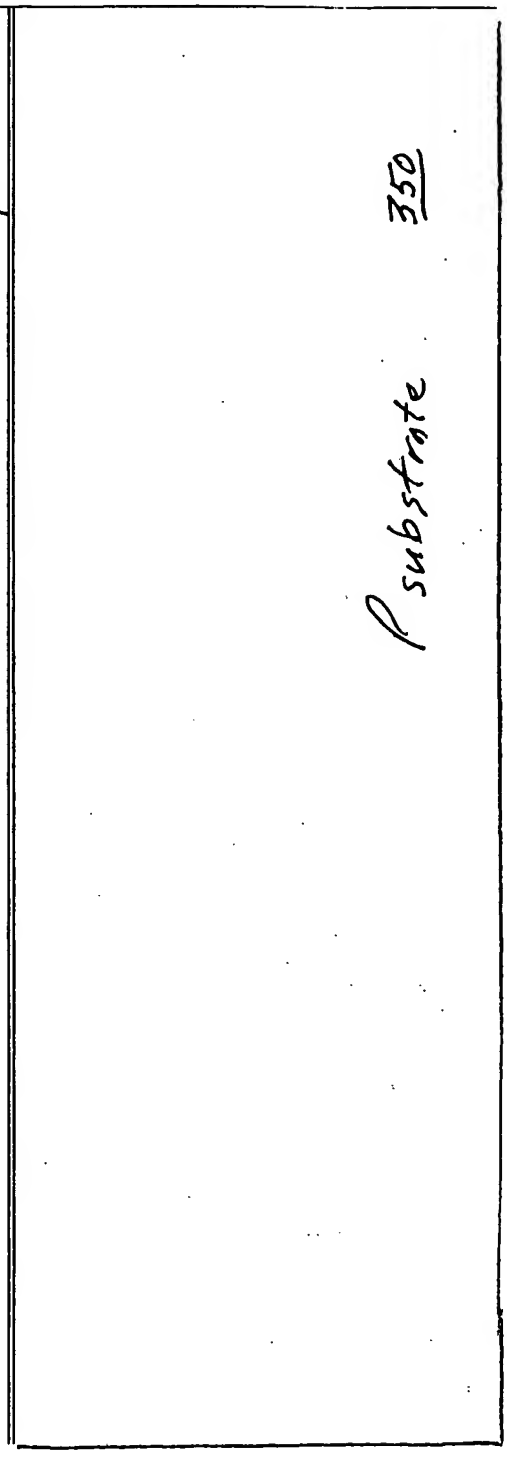
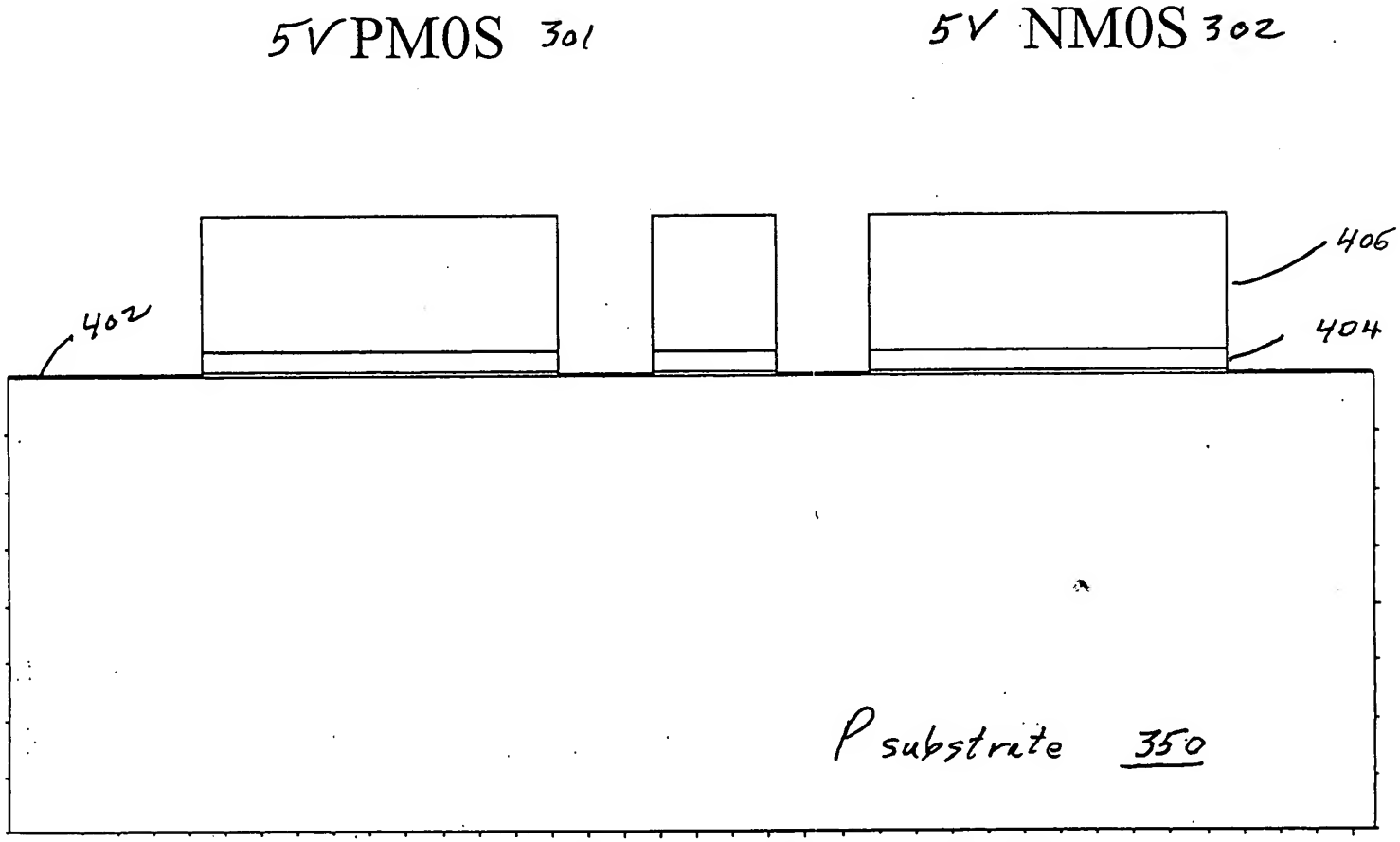


Fig. 21



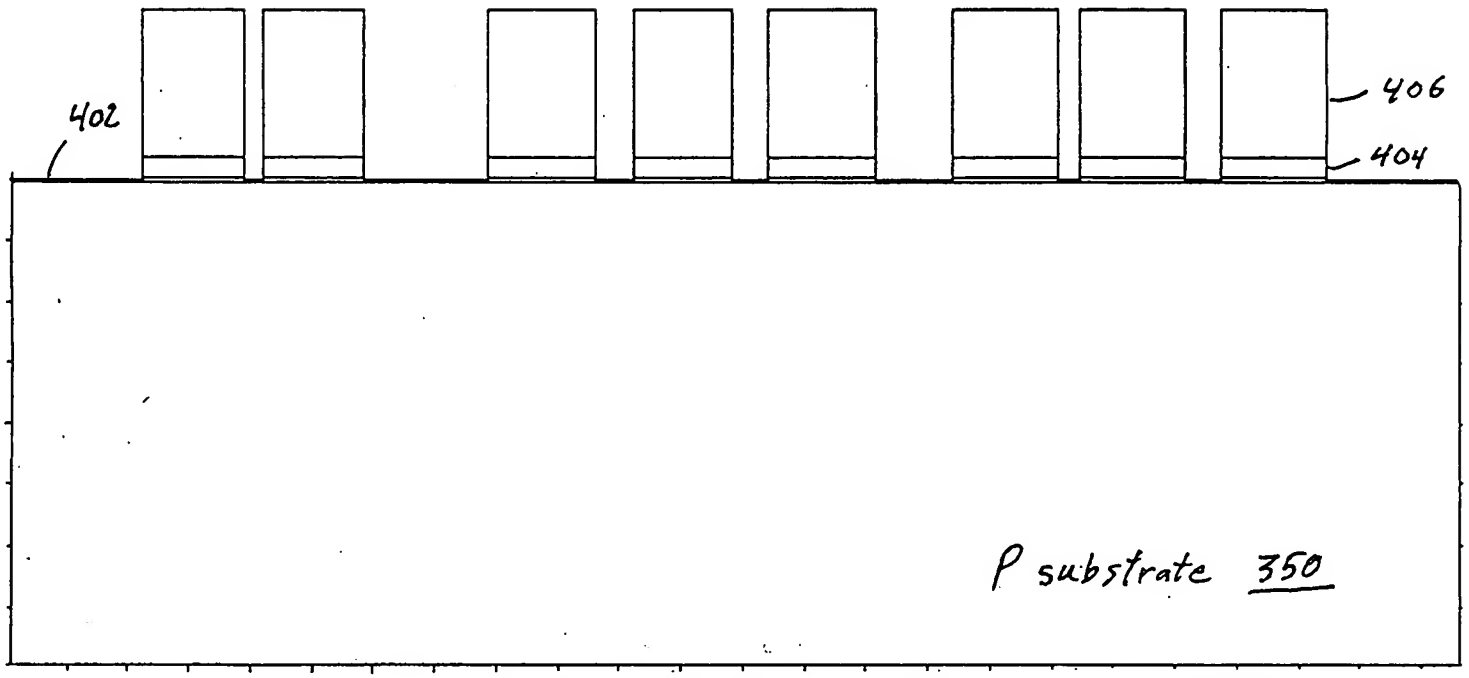
LOCOS - Nitride Mask and Etch

Fig. 22A

High F_T Layout

5V NPN 305

5V PNP 306



Locos – Nitride Mask and Etch

Fig. 22B

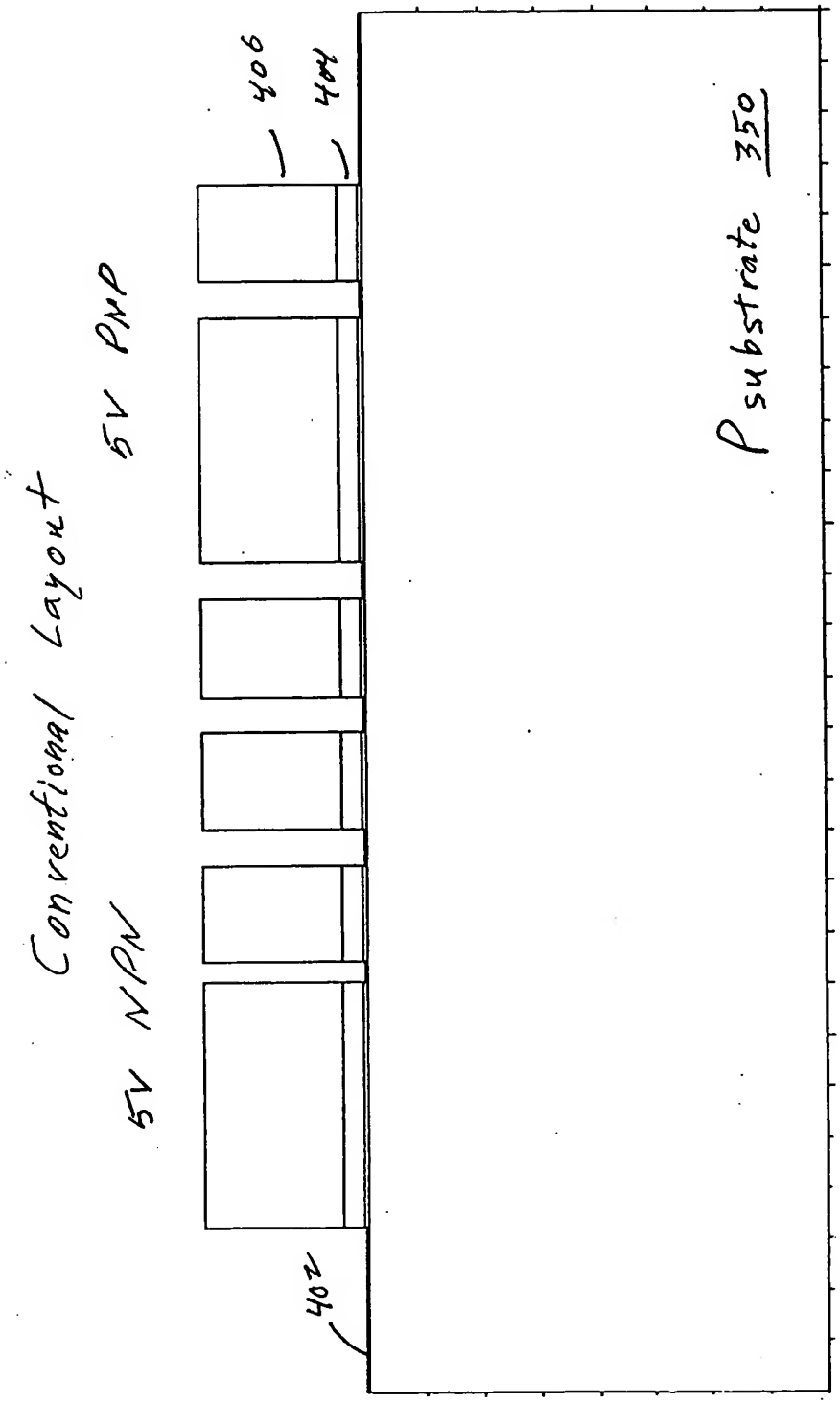

406
404
5V PMP
Conventional Layout
5V NPN
402
P substrate 350
LOCOS - Nitride Mask and Etch

Fig. 22C

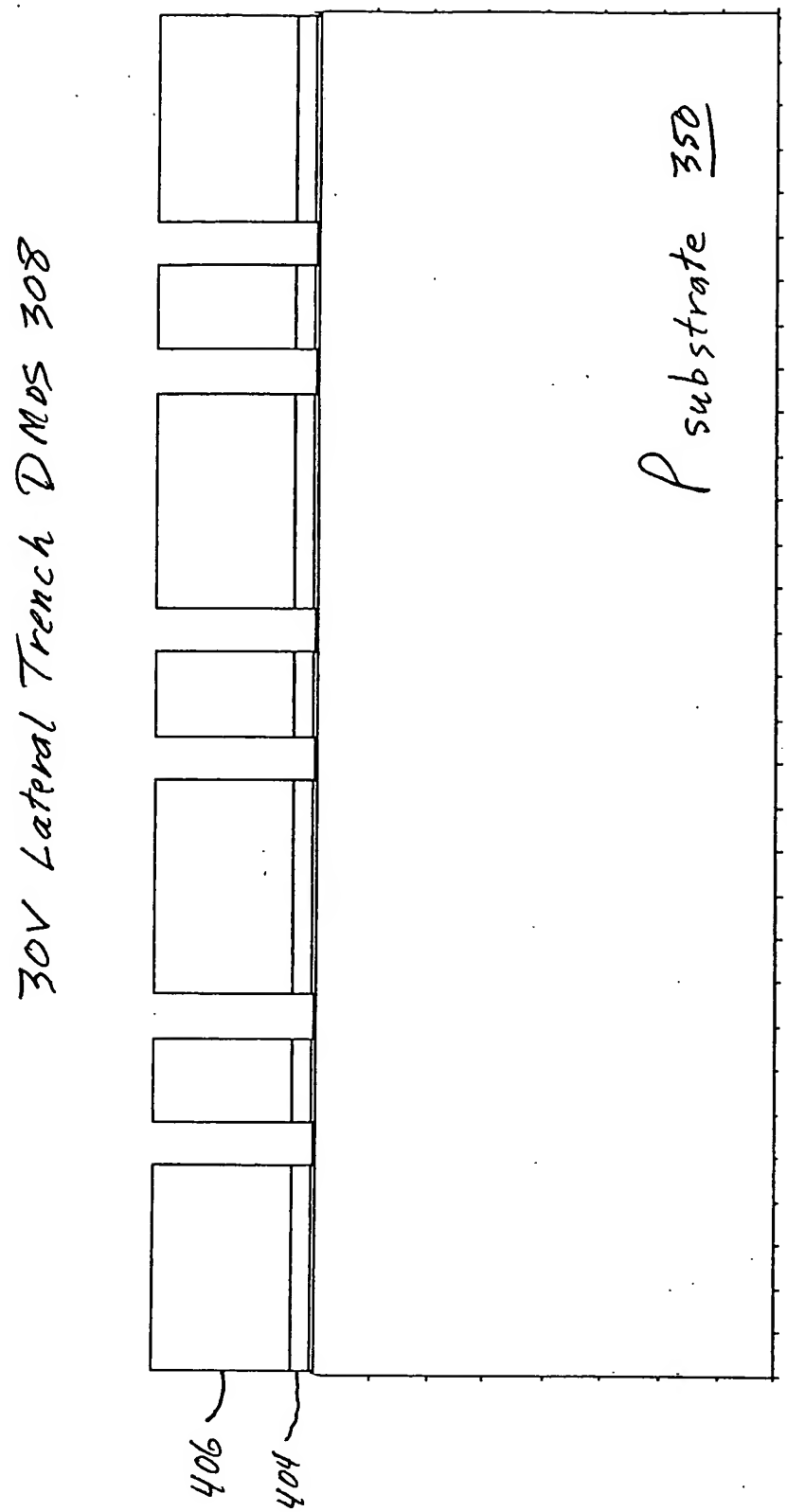
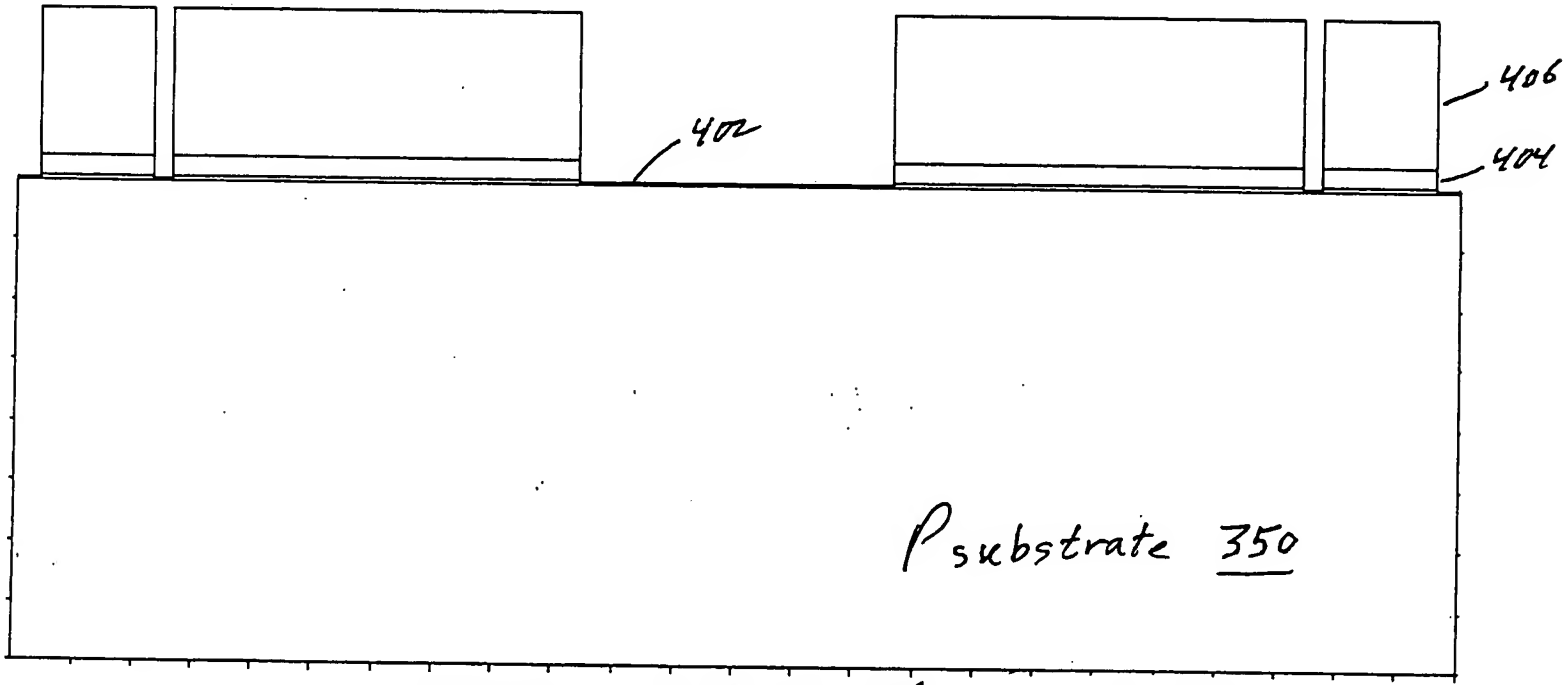

30V Lateral Trench DMOS 308
P substrate 350
LOCOS - Nitride Mask and Etch
406
404

Fig. 22D

Symmetrical 12V CMOS

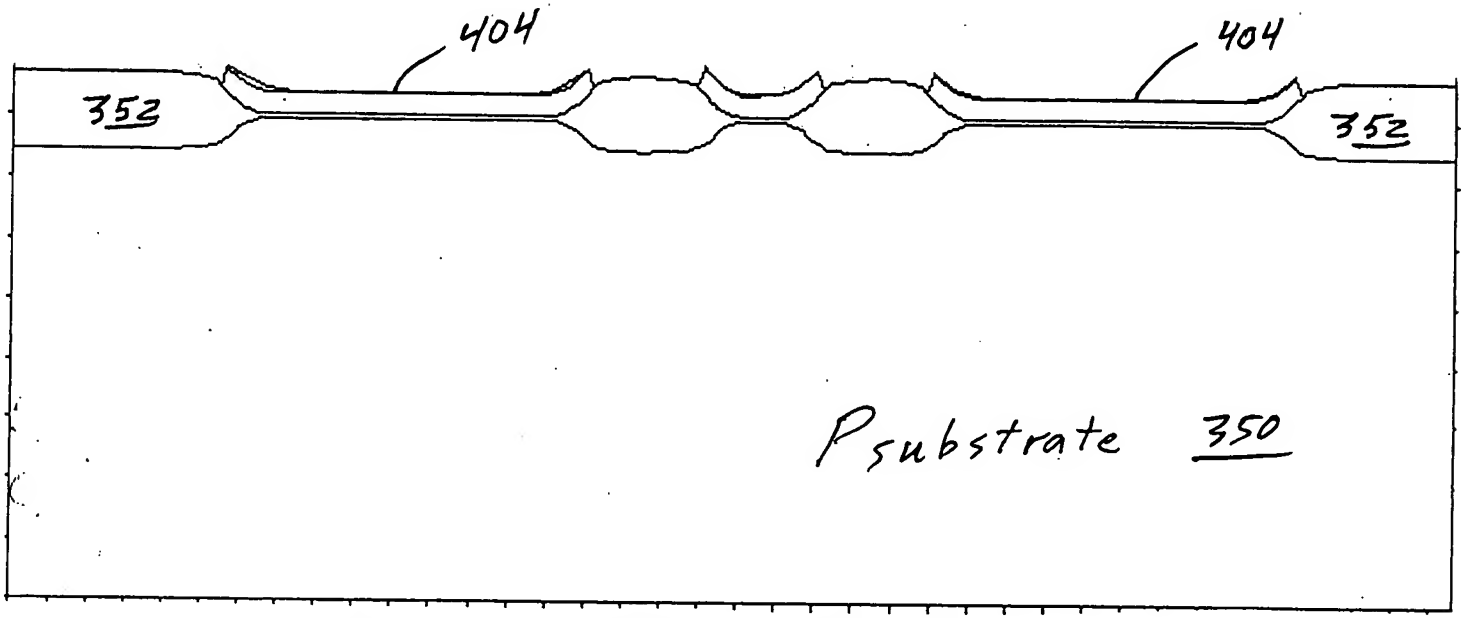
12V PMOS 309 12V NMOS 310



LOCOS – Nitride Mask and Etch

Fig. 22E

5V PMOS 301 5V NMOS 302



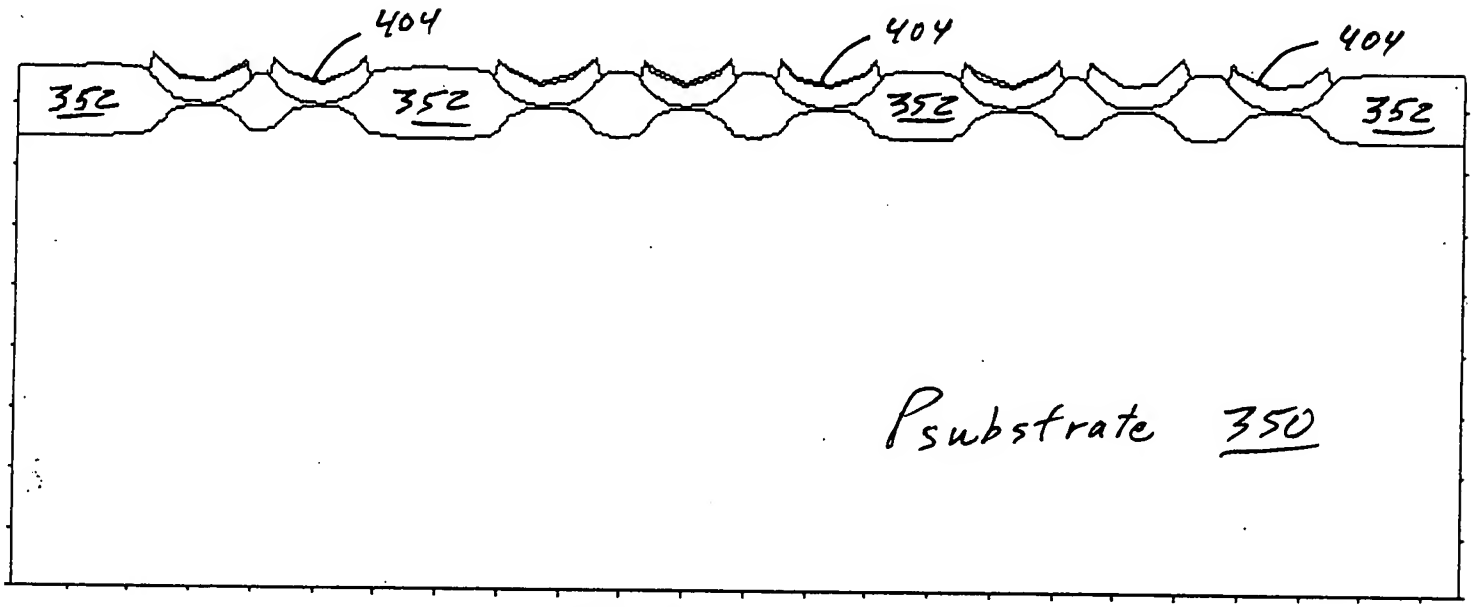
LOCOS – Field Oxidation

Fig. 23A

High F_T Layout

5V NPN 305

5V PNP 306

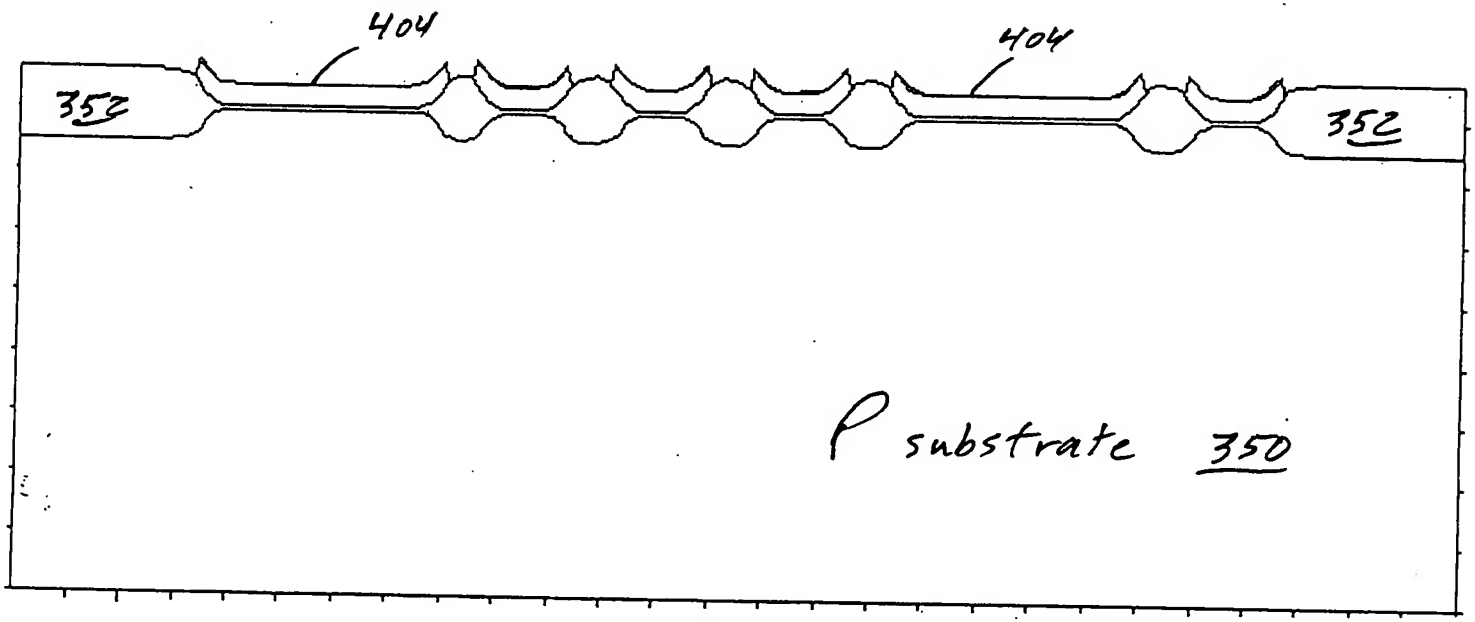


LOCOS - Field Oxidation

Fig. 23B

Conventional Layout

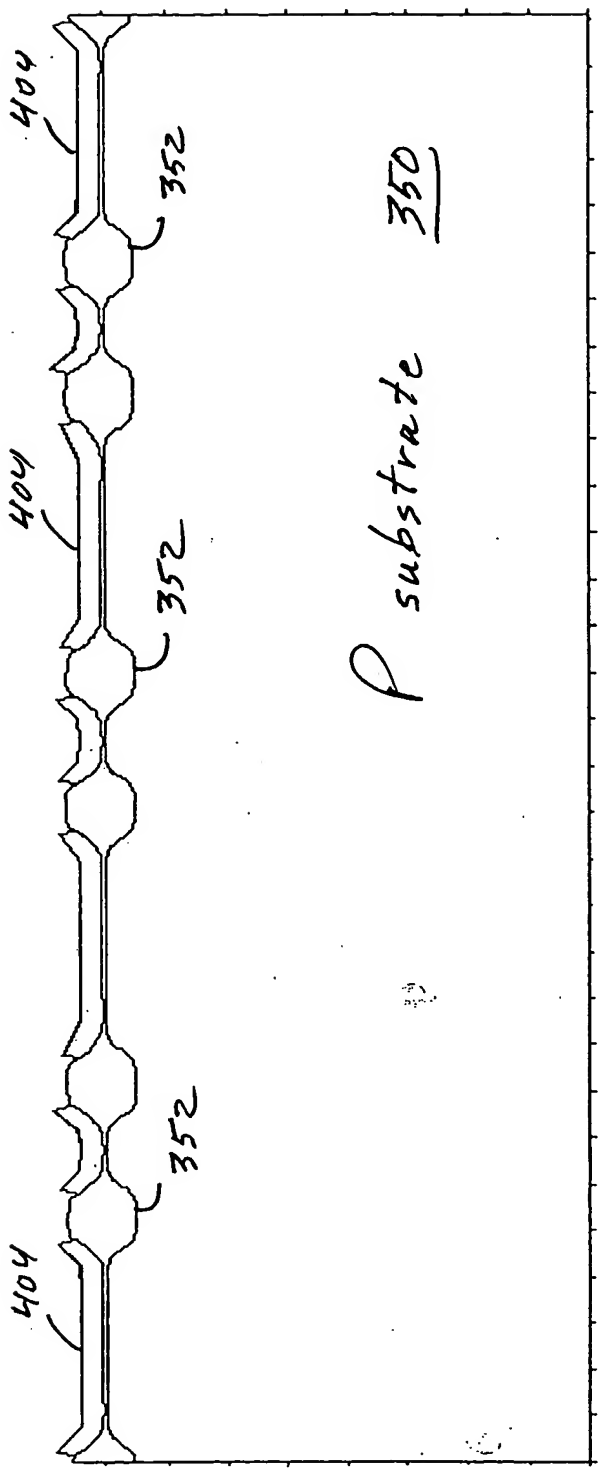
5V NPN 5V PNP



LOCOS - Field Oxidation

Fig 23C

30V Lateral Trench DMOS

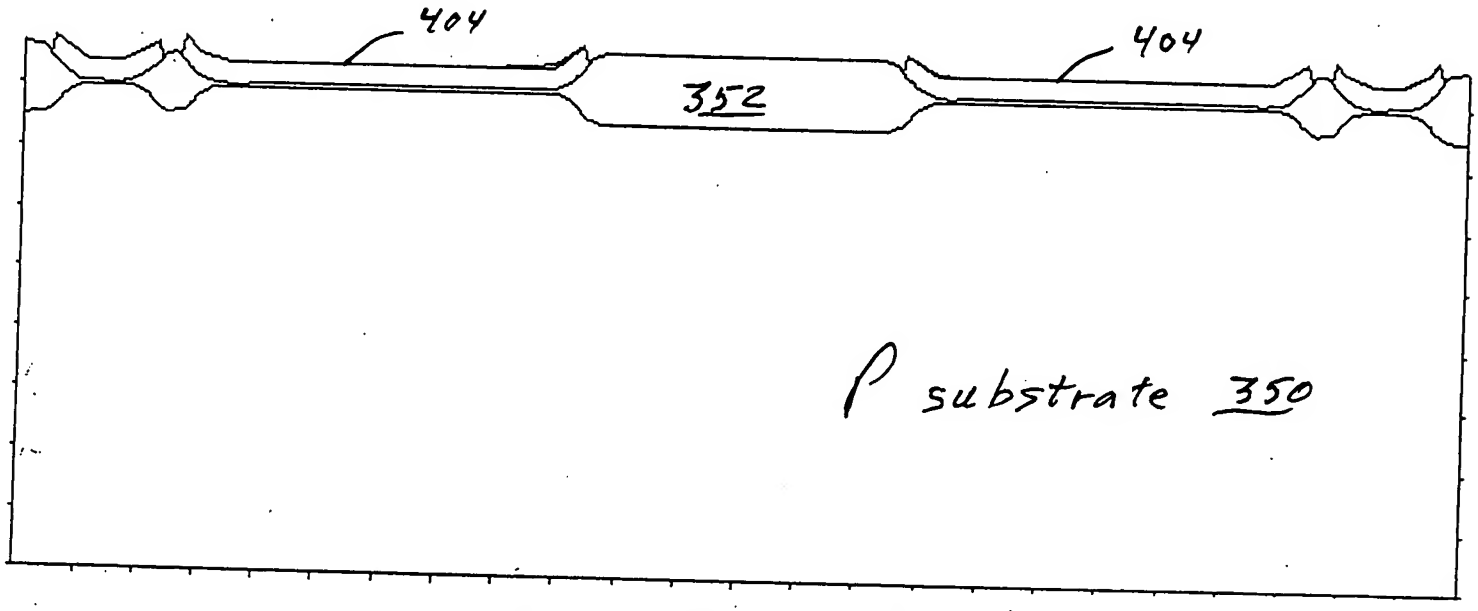


LOCOS - Field Oxidation

Fig. 23D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

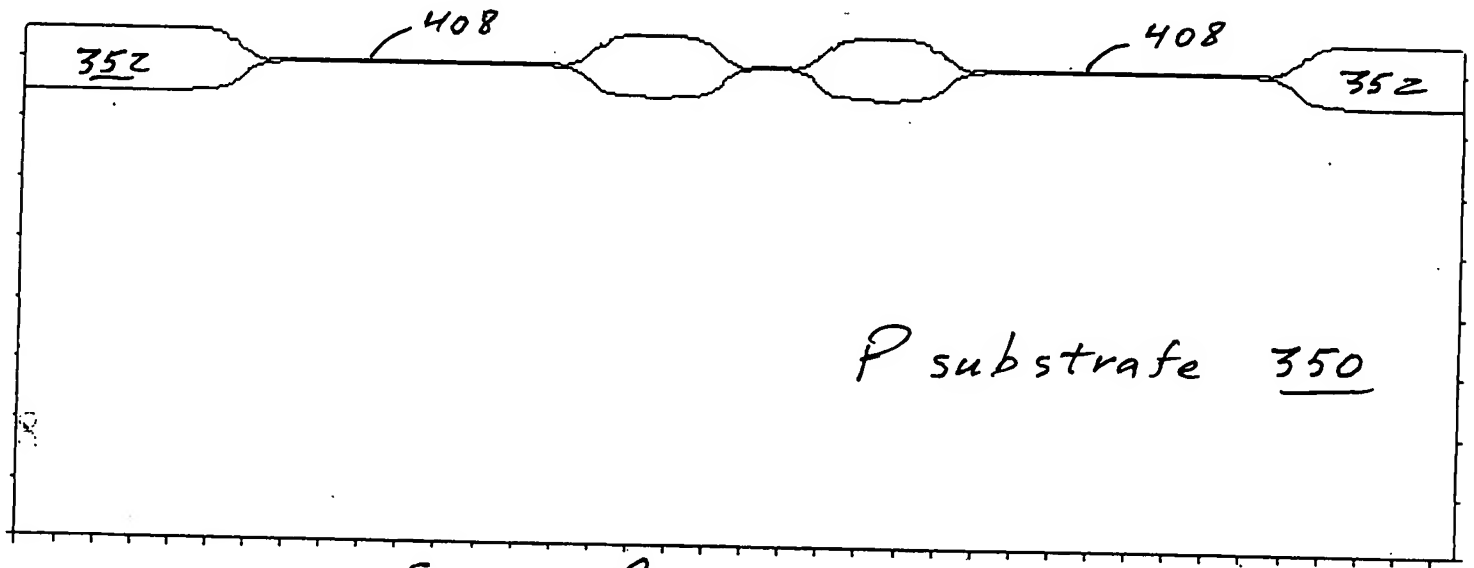


LOCOS - Field Oxidation

Fig. 23E

5V PMOS 301

5V NMOS 302



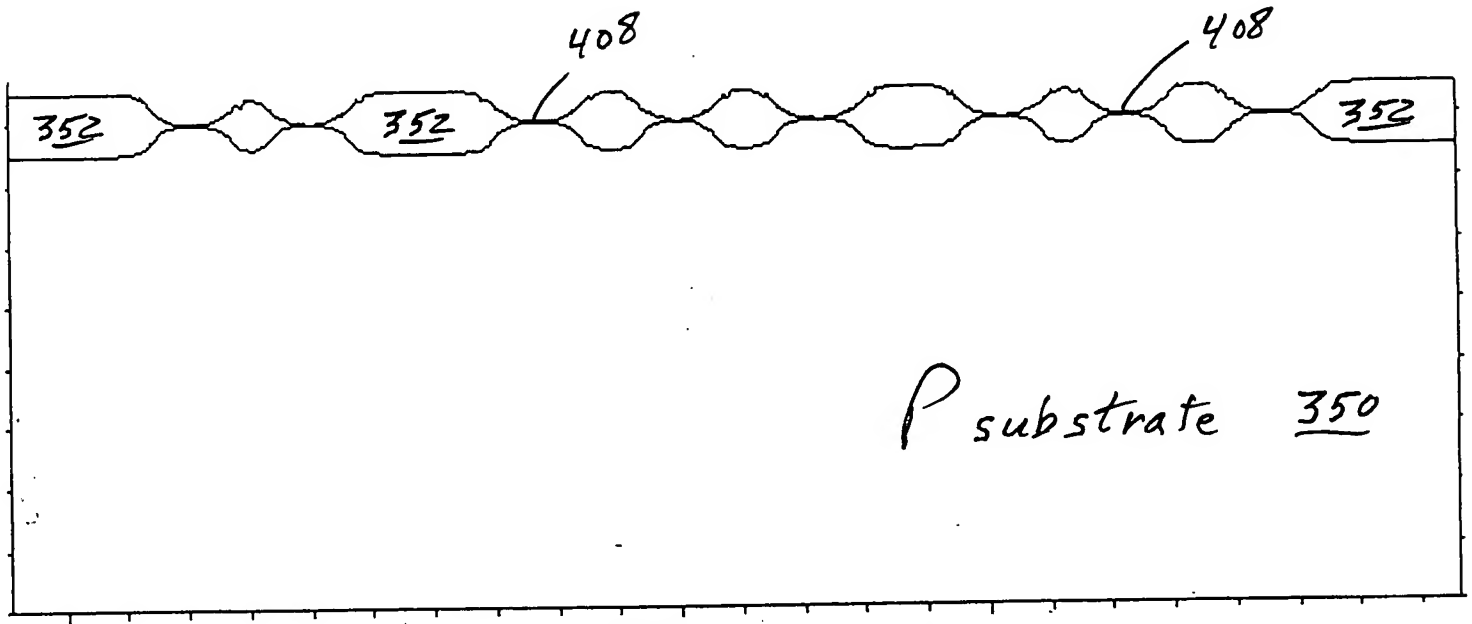
Second Pad Oxide Layer

Fig. 24A

High F_T Layout

5V NPN 305

5V PNP 306



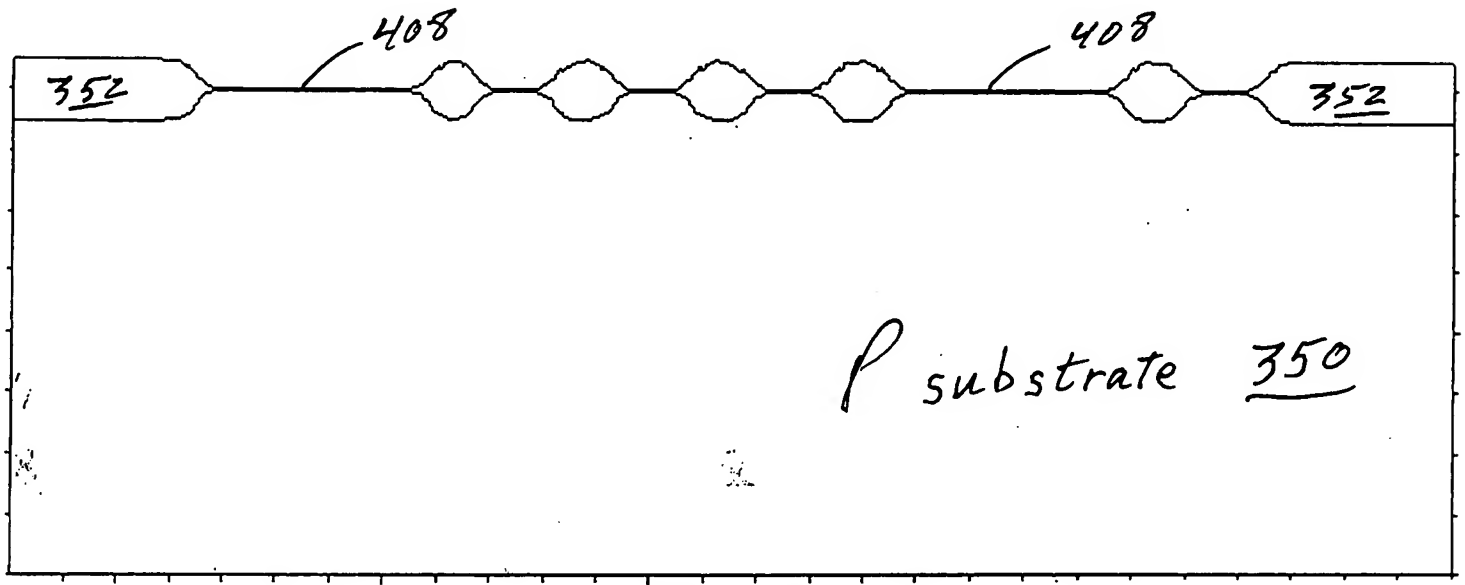
Second Pad Oxide Layer

Fig. 24B

Conventional Layout

5V NPN

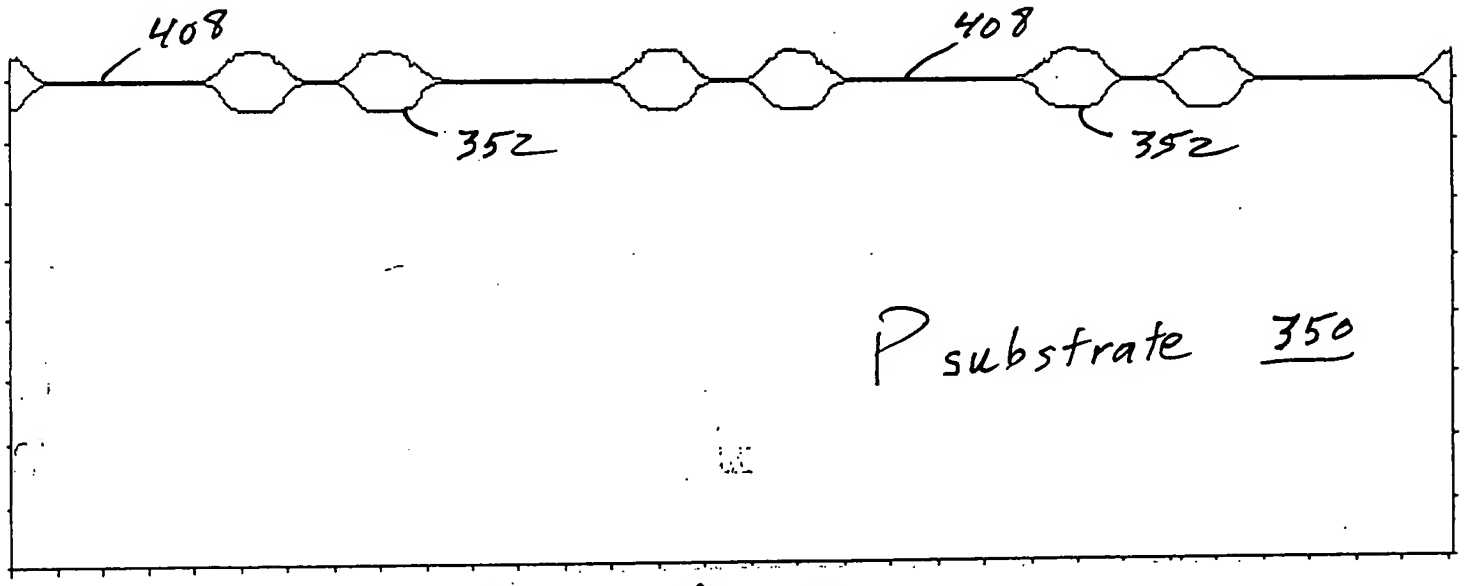
5V PNP



Second Pad Oxide Layer

Fig. 24C

30V Lateral Trench DMOS 308

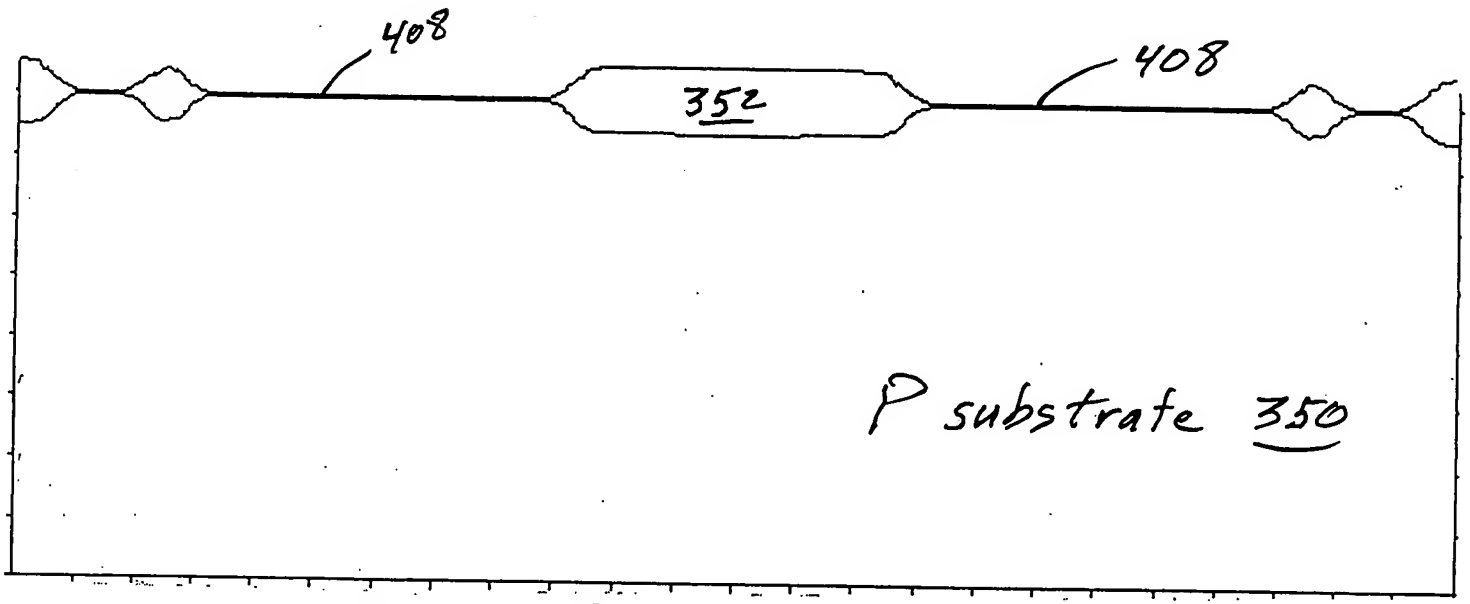


Second Pad Oxide Layer

Fig 24D

Symmetrical 12V CMOS

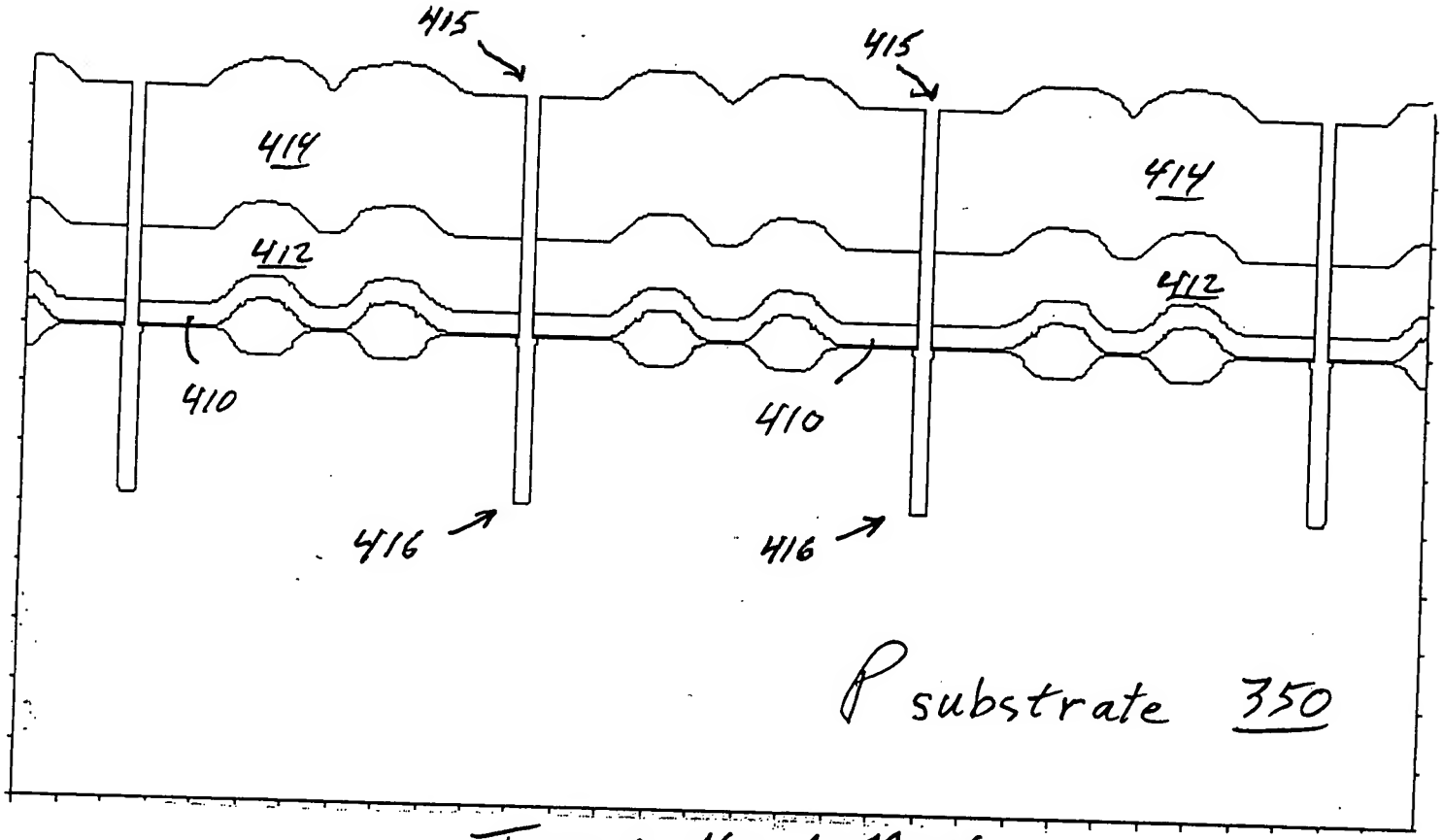
12V PMOS 309 12V NMOS 310



Second Pad Oxide Layer

Fig. 24E

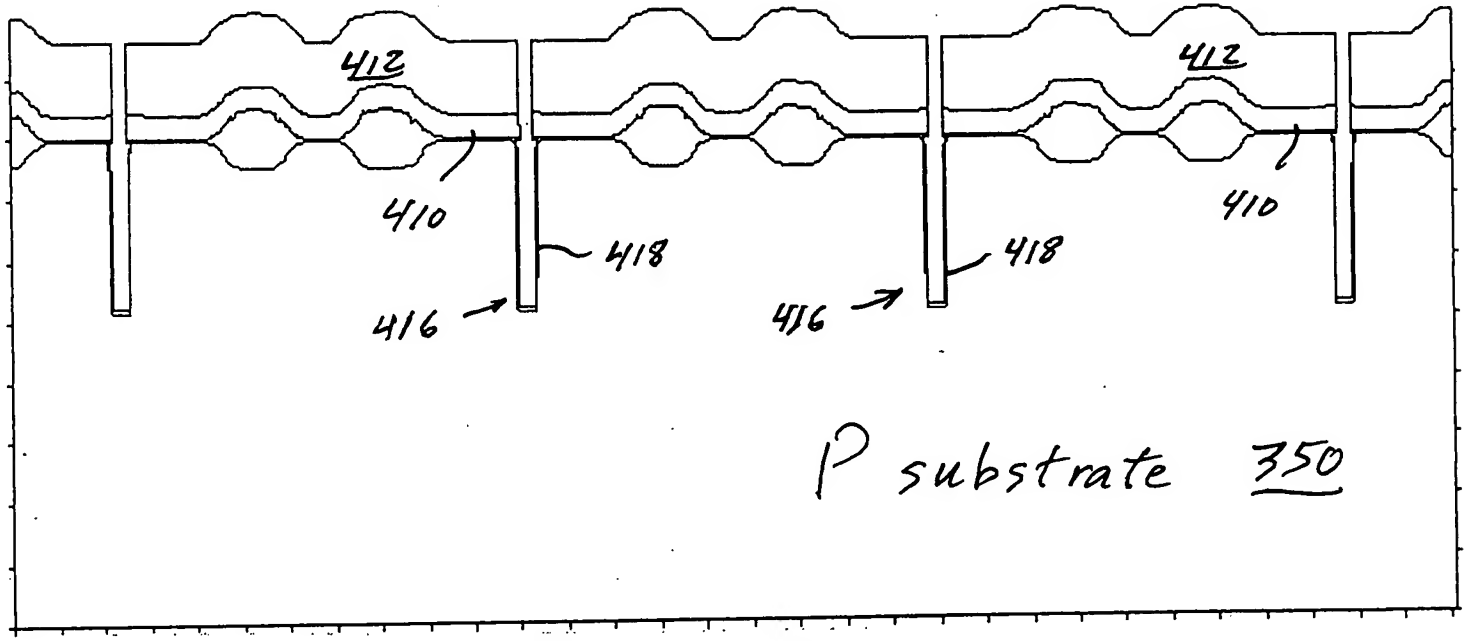
30V Lateral Trench DMOS 308



Trench Hard Mask

Fig. 25D

30V Lateral Trench DMOS 308



Sacrificial Oxide

Fig. 26D

30 V Lateral Trench DMOS 308

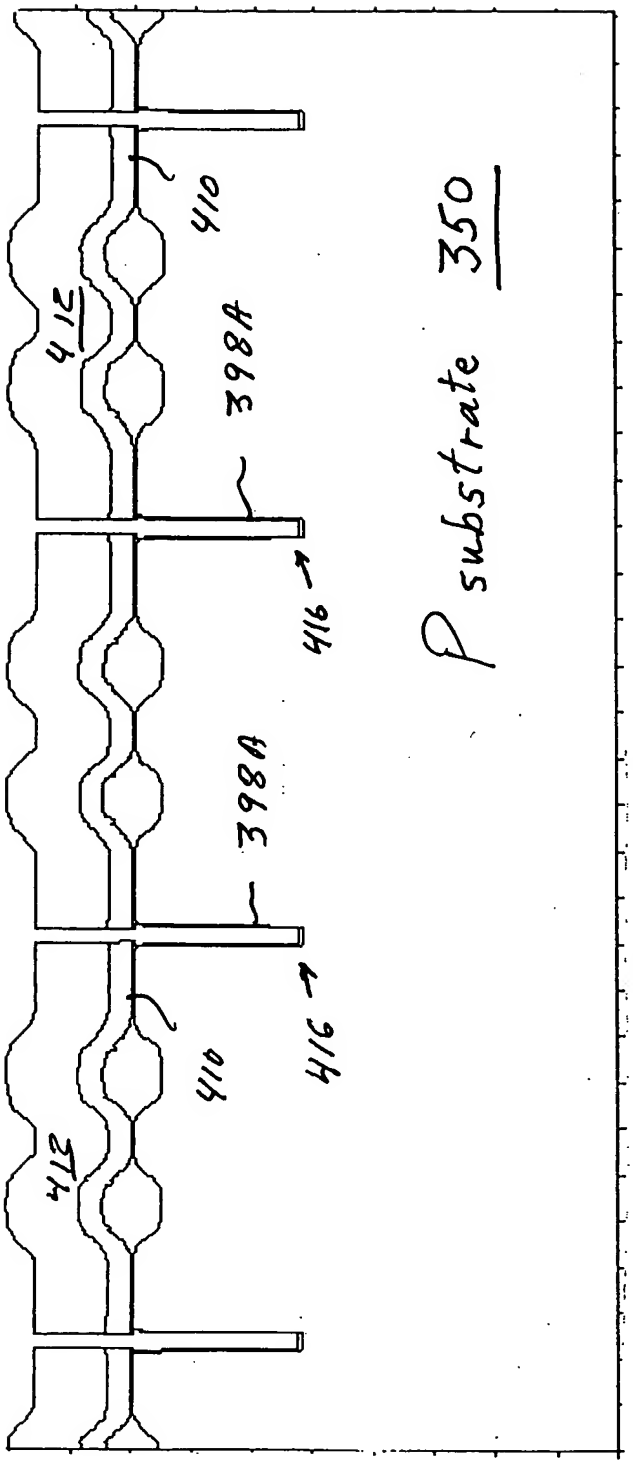
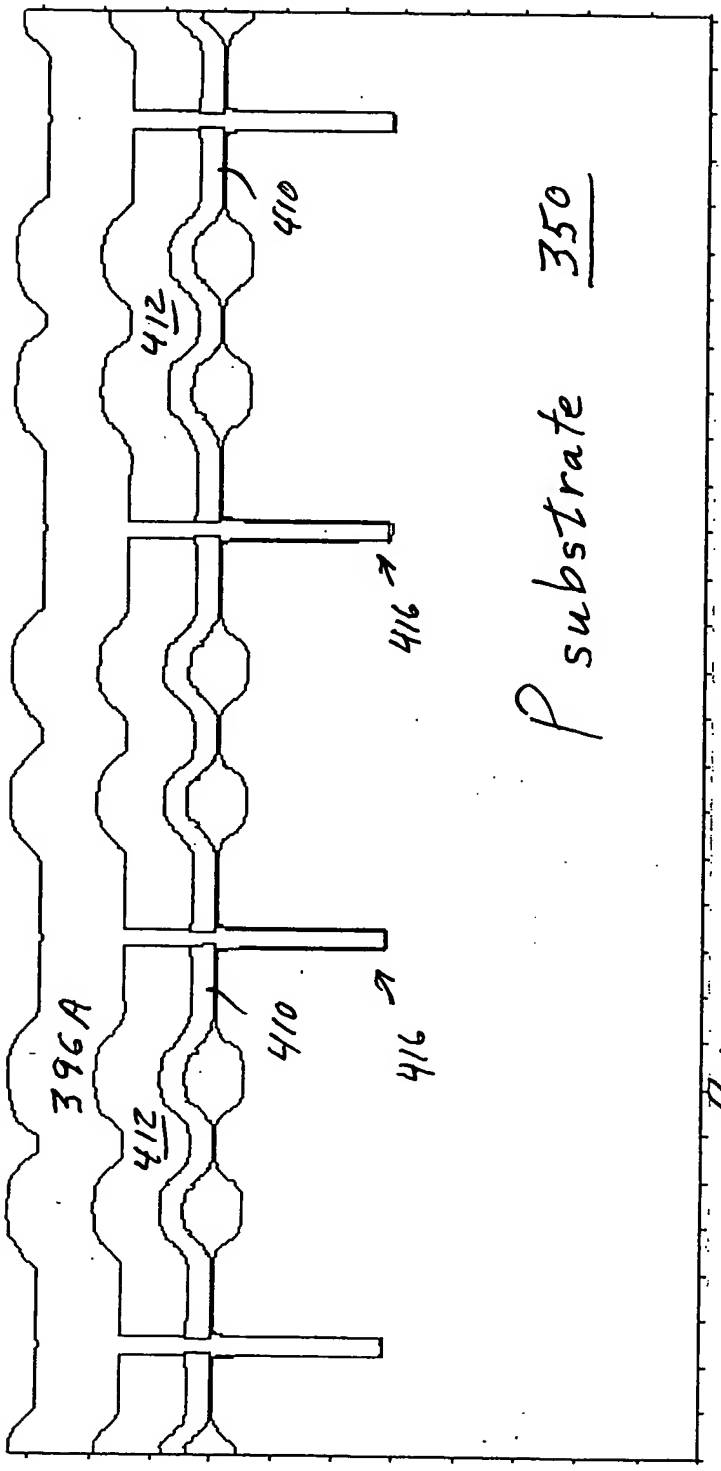


Fig. 27D

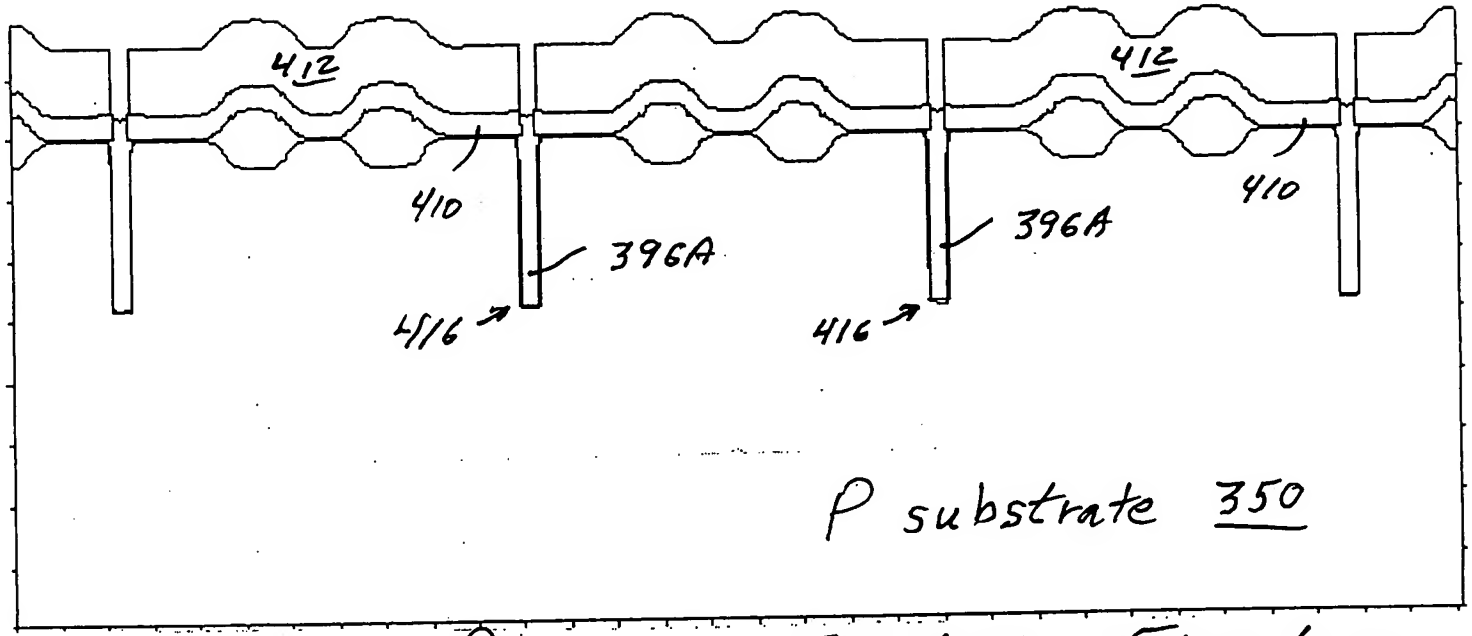
30 V Lateral Trench DMOS 308



Polysilicon - First Layer

Fig 28D

30V Lateral Trench DMOS 308



Polysilicon Etchback - First Layer

Fig. 29D

30V Lateral Trench DMOS 308

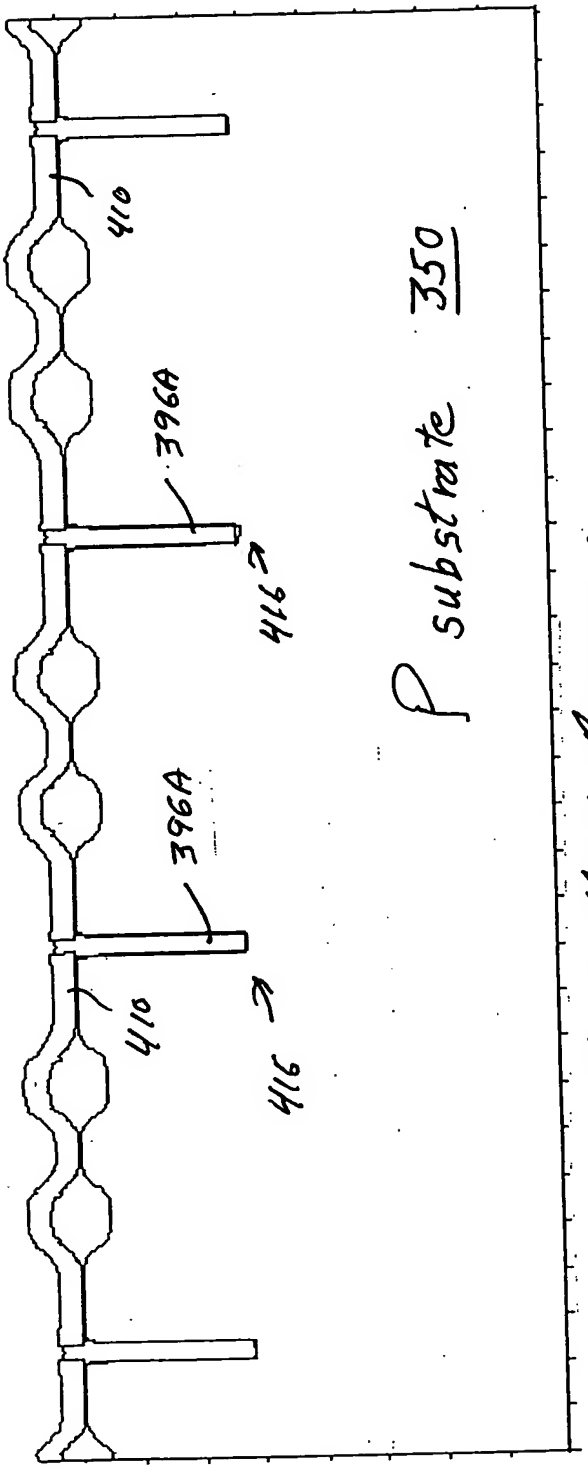
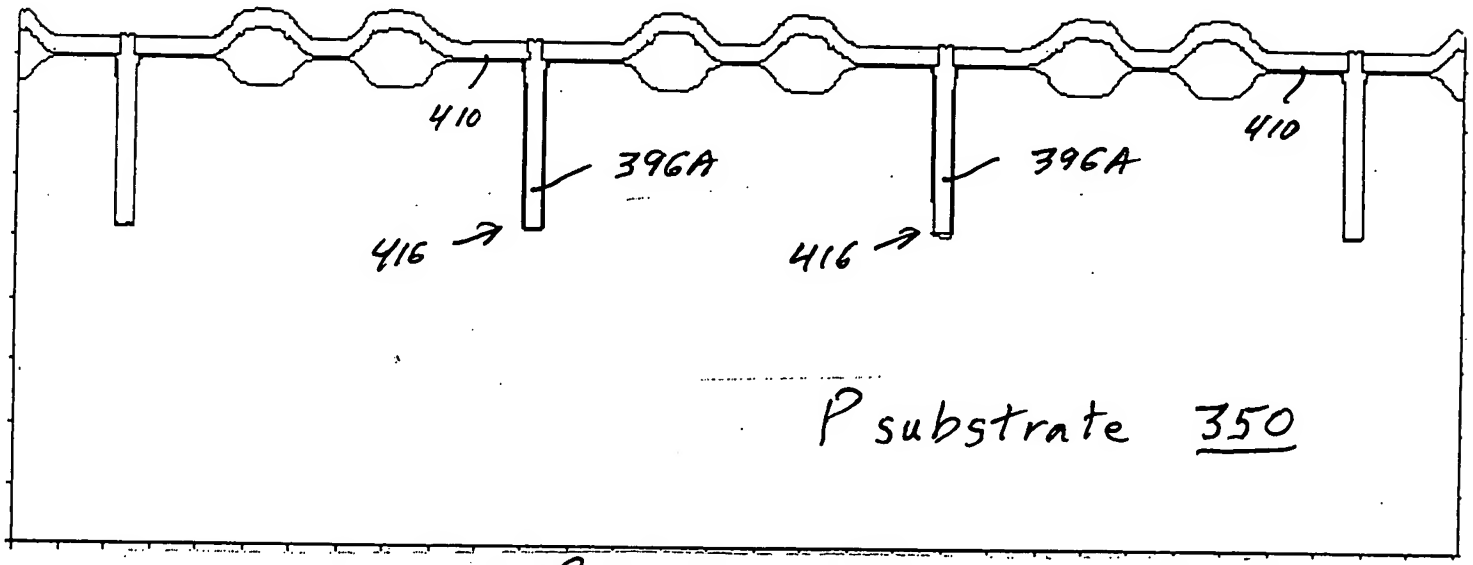


Fig. 30D

- 30V Lateral Trench DMOS 308



Second Polysilicon Etchback – First Layer

Fig. 31D

30V Lateral Trench DMOS 308

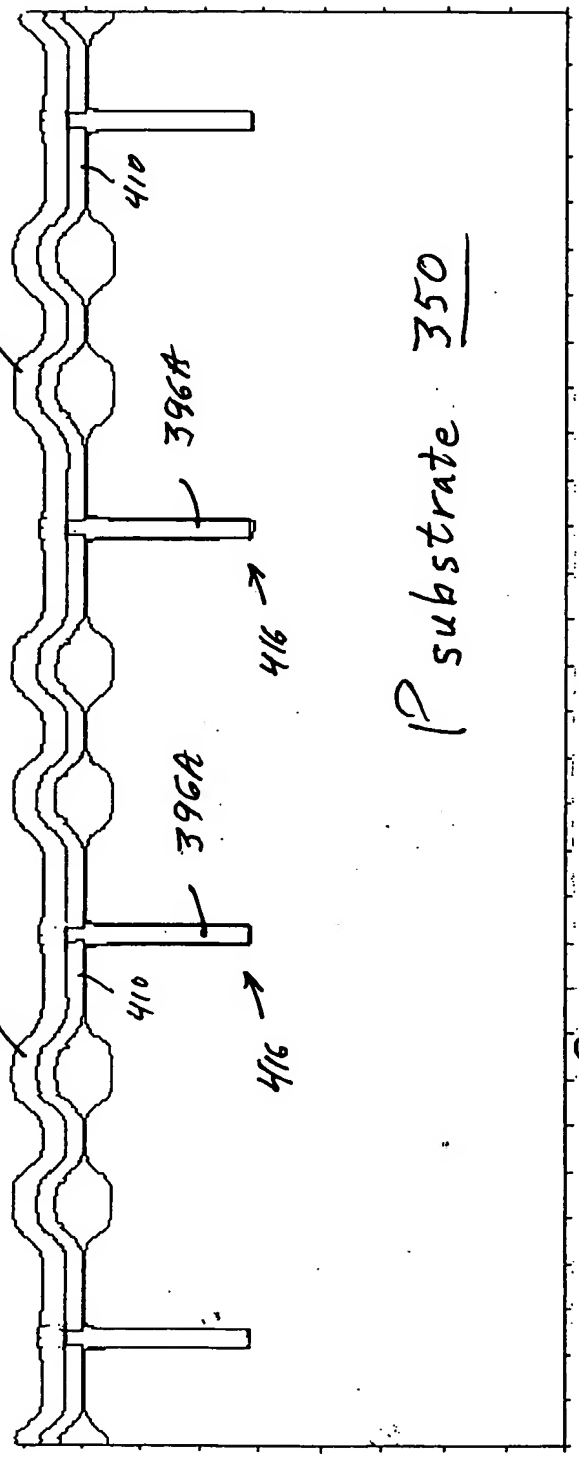


Fig. 32D

30V Lateral Trench DMOS 308

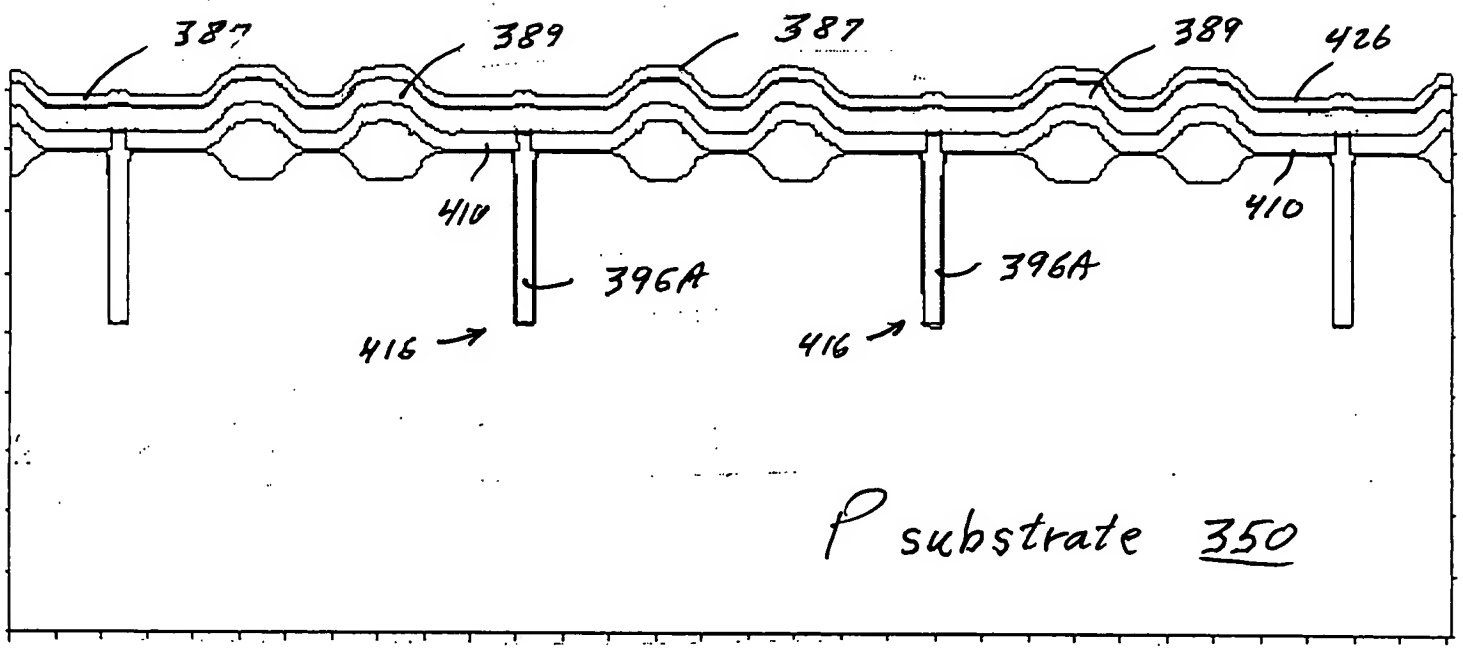
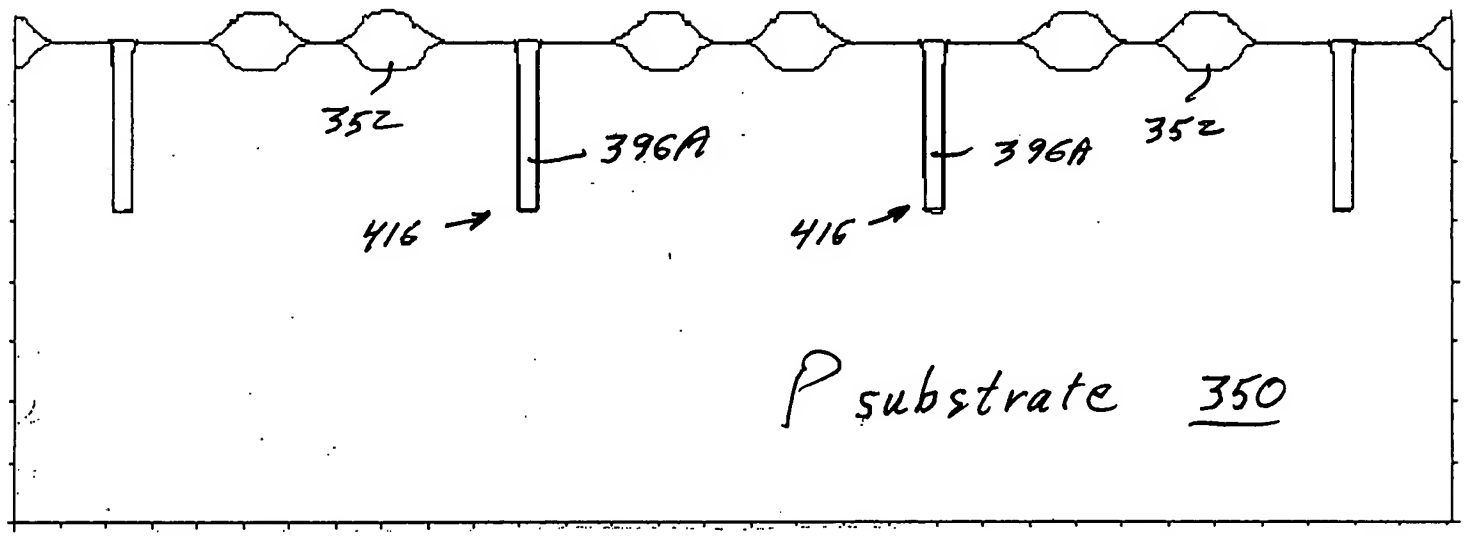


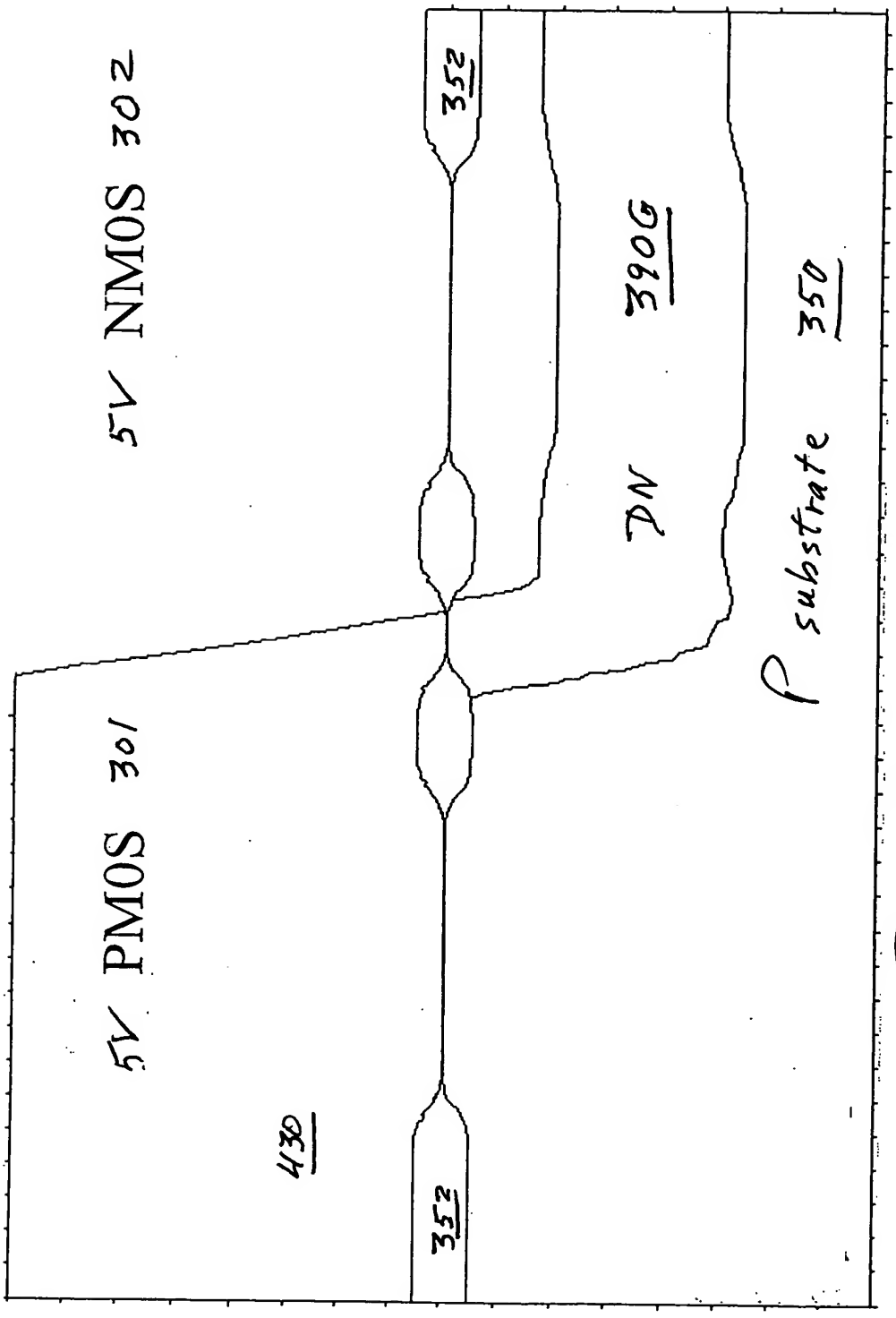
Fig 33D

30 V Lateral Trench DMOS 308



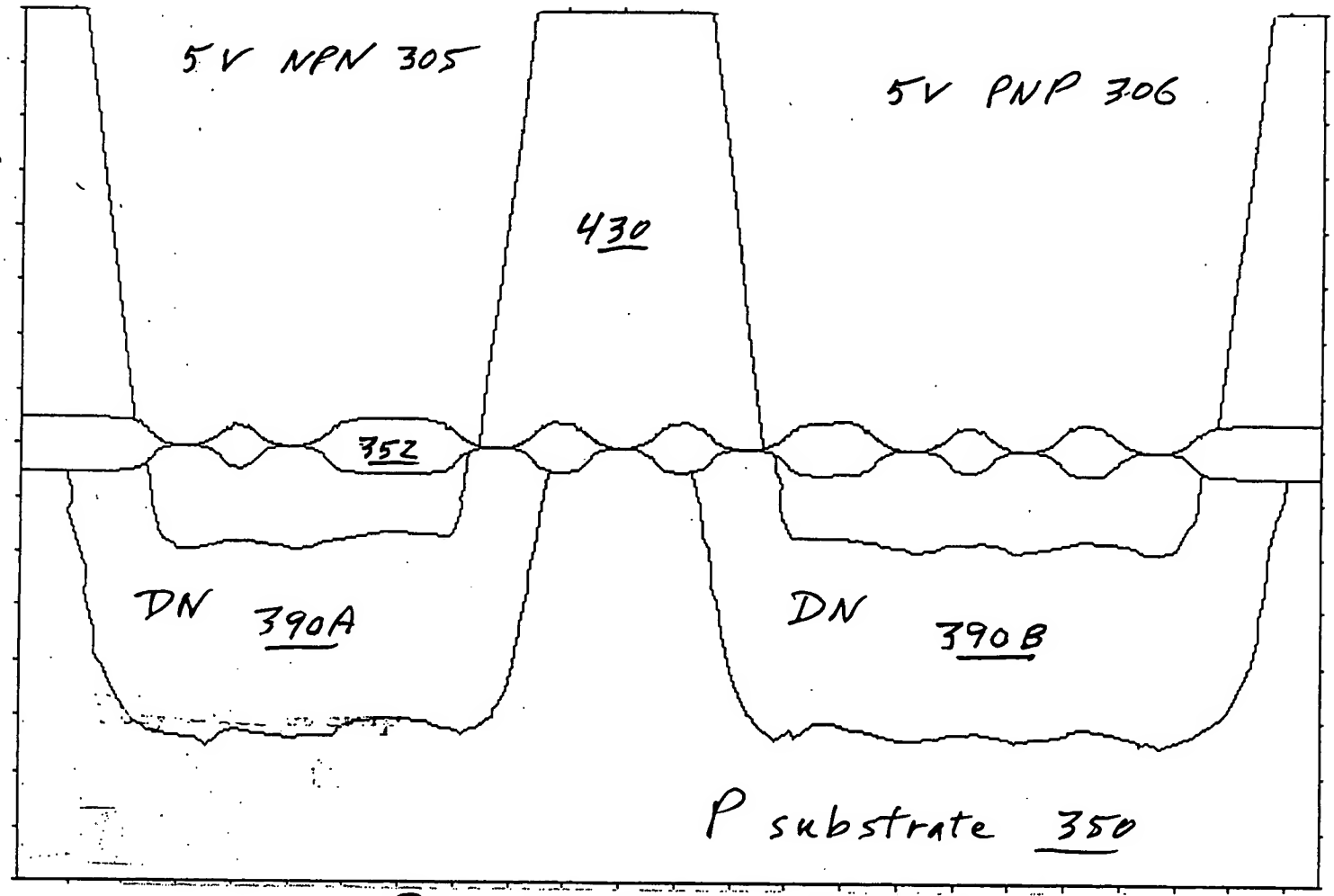
Etchback - Interlayer Dielectric and Second Poly

Fig. 34D



Deep N Mask and Implant
Fig. 3SA

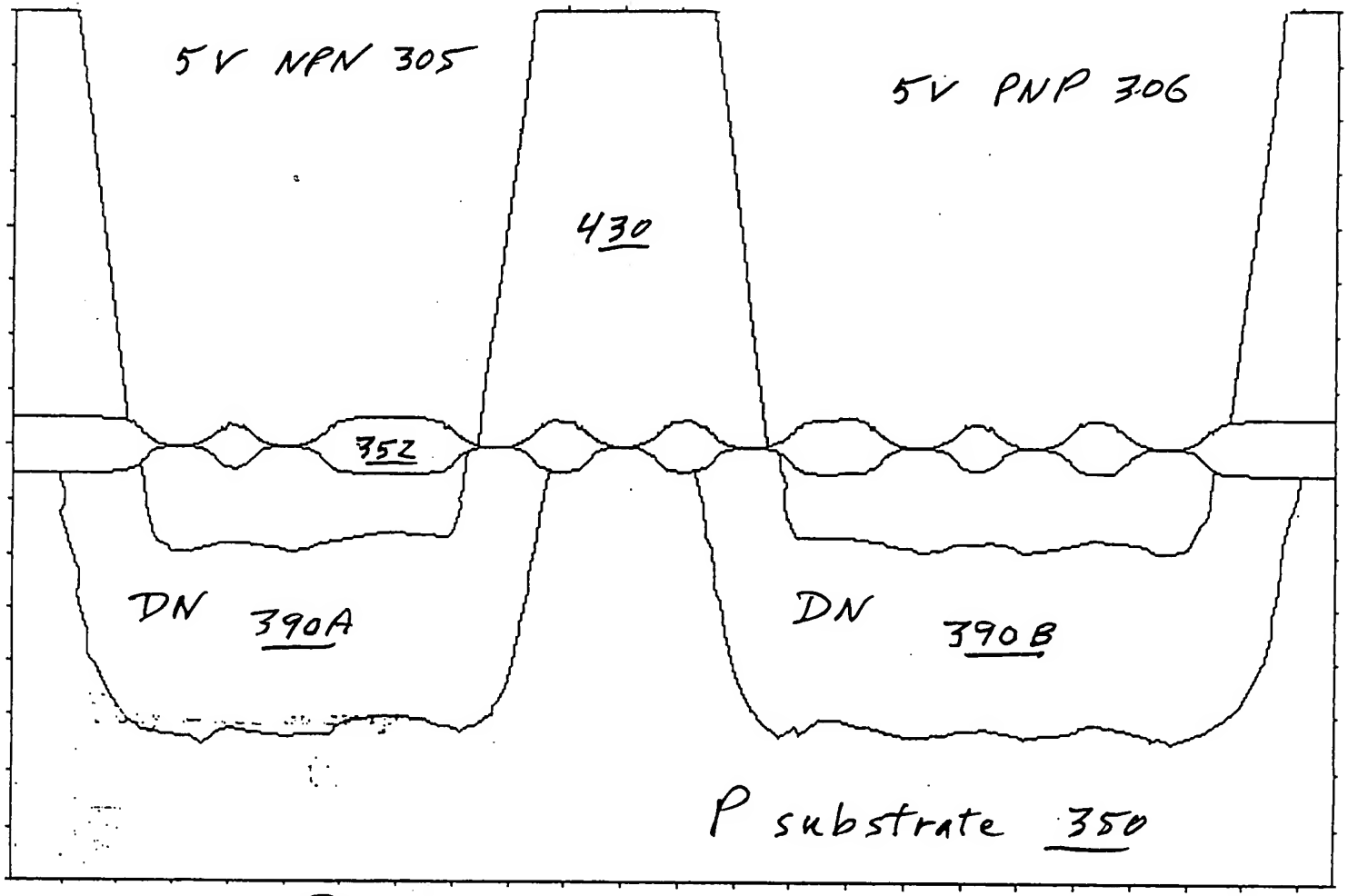
High F_T Layout



Deep N Mask and Implant

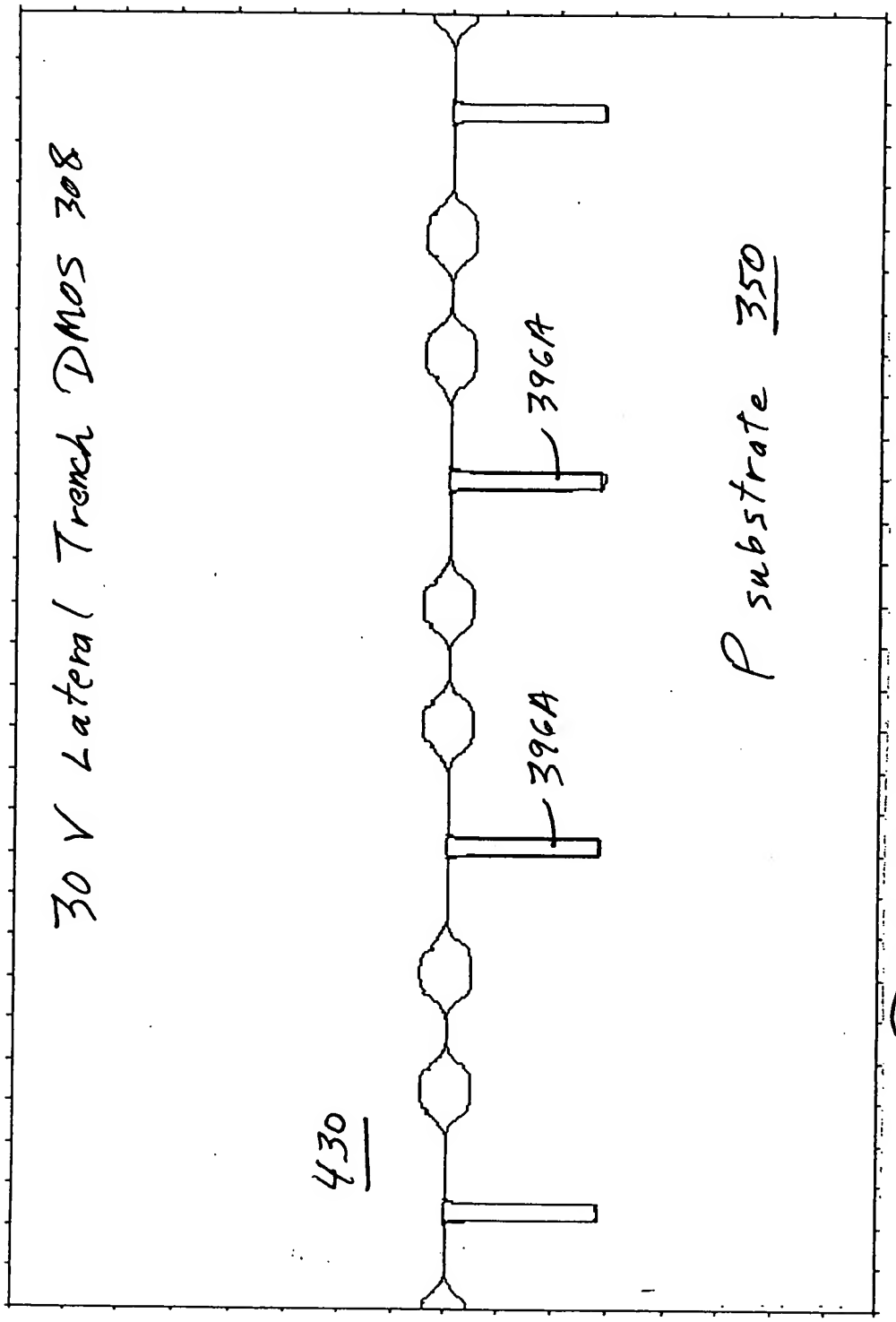
Fig 35B

Conventional Layout

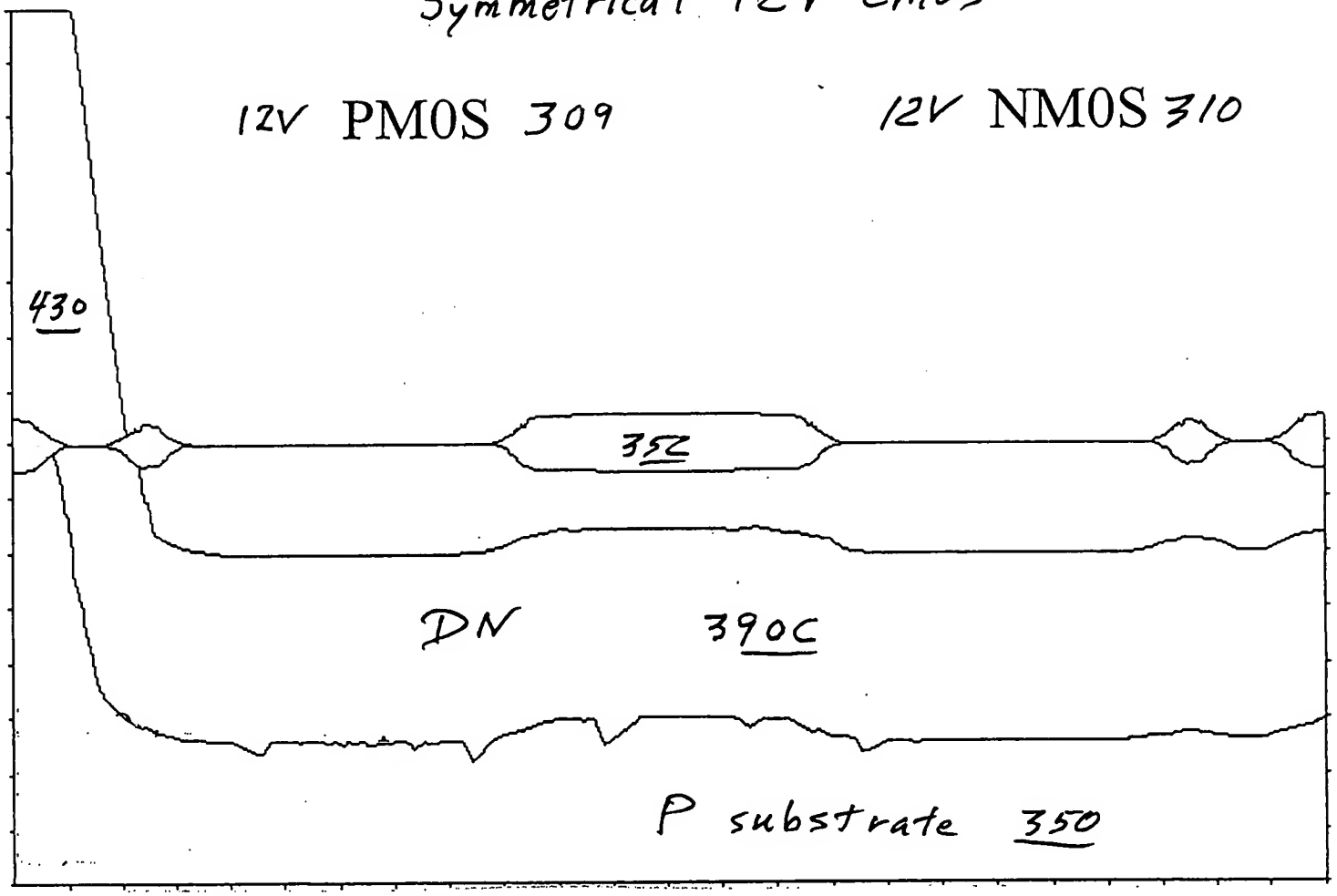


Deep N Mask and Implant

Fig. 35C



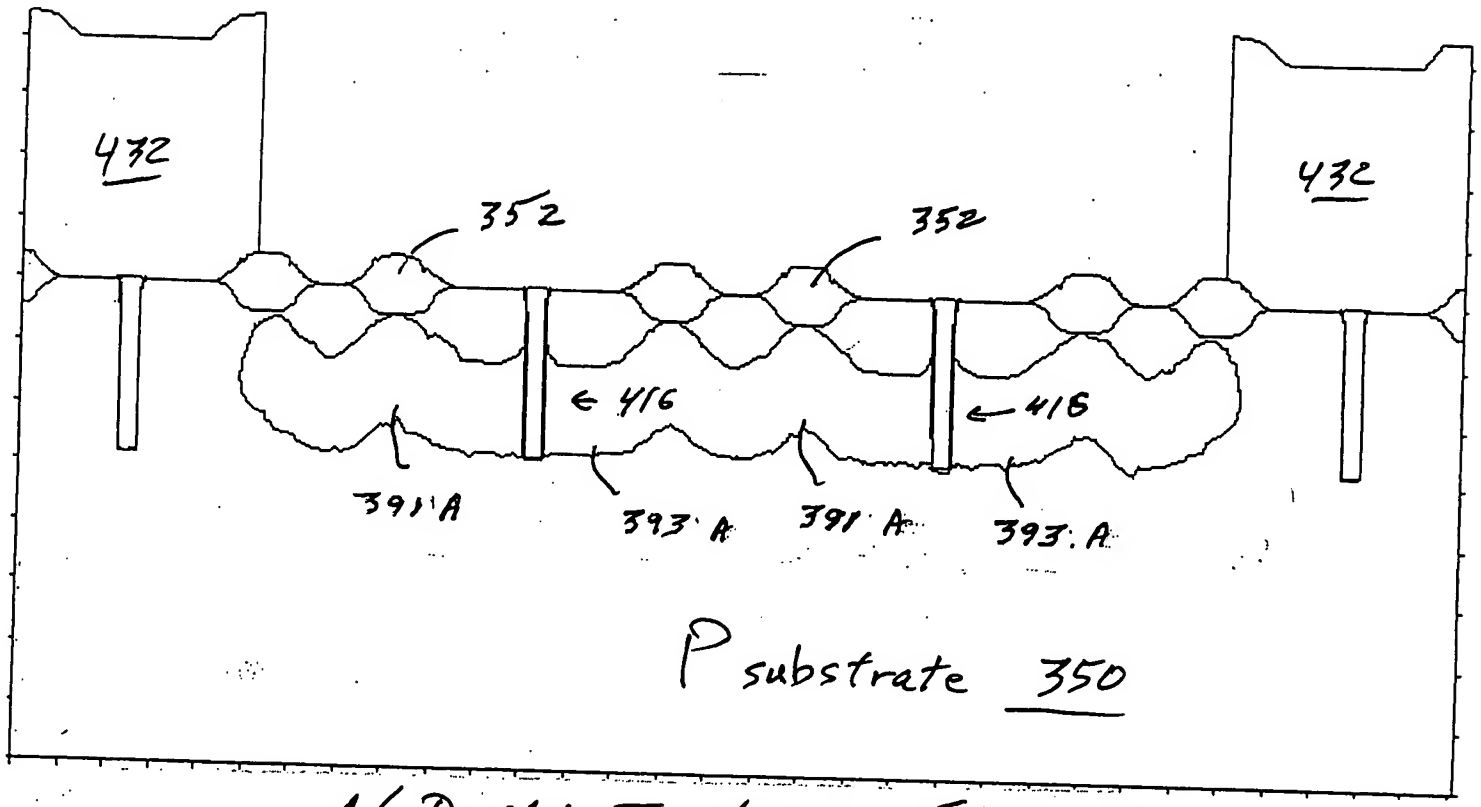
Deep N Mask and Implant
Fig. 35D



Deep N Mask and Implant

Fig. 35E

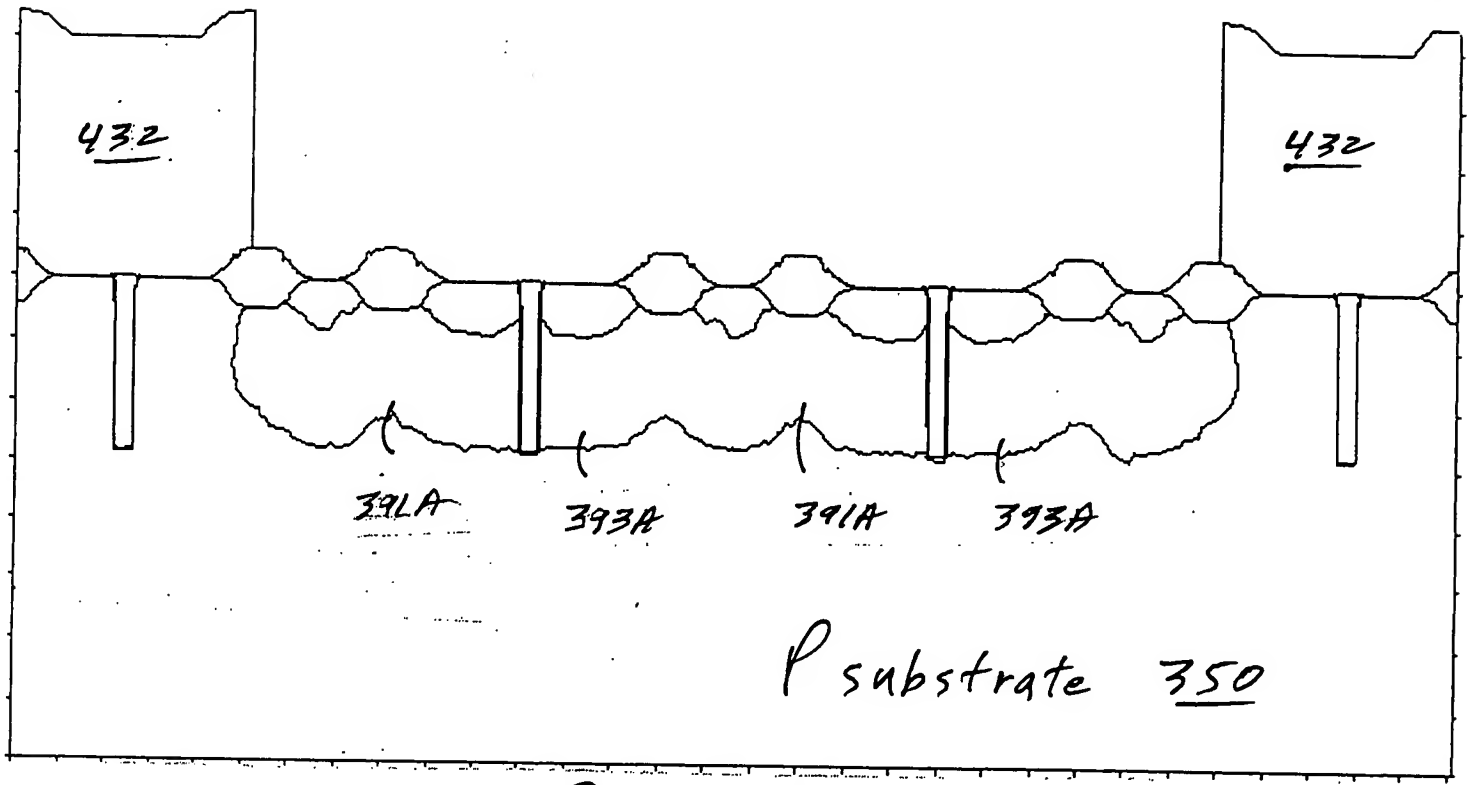
30 V Lateral Trench DMOS 308



N Drift Implant - First Stage

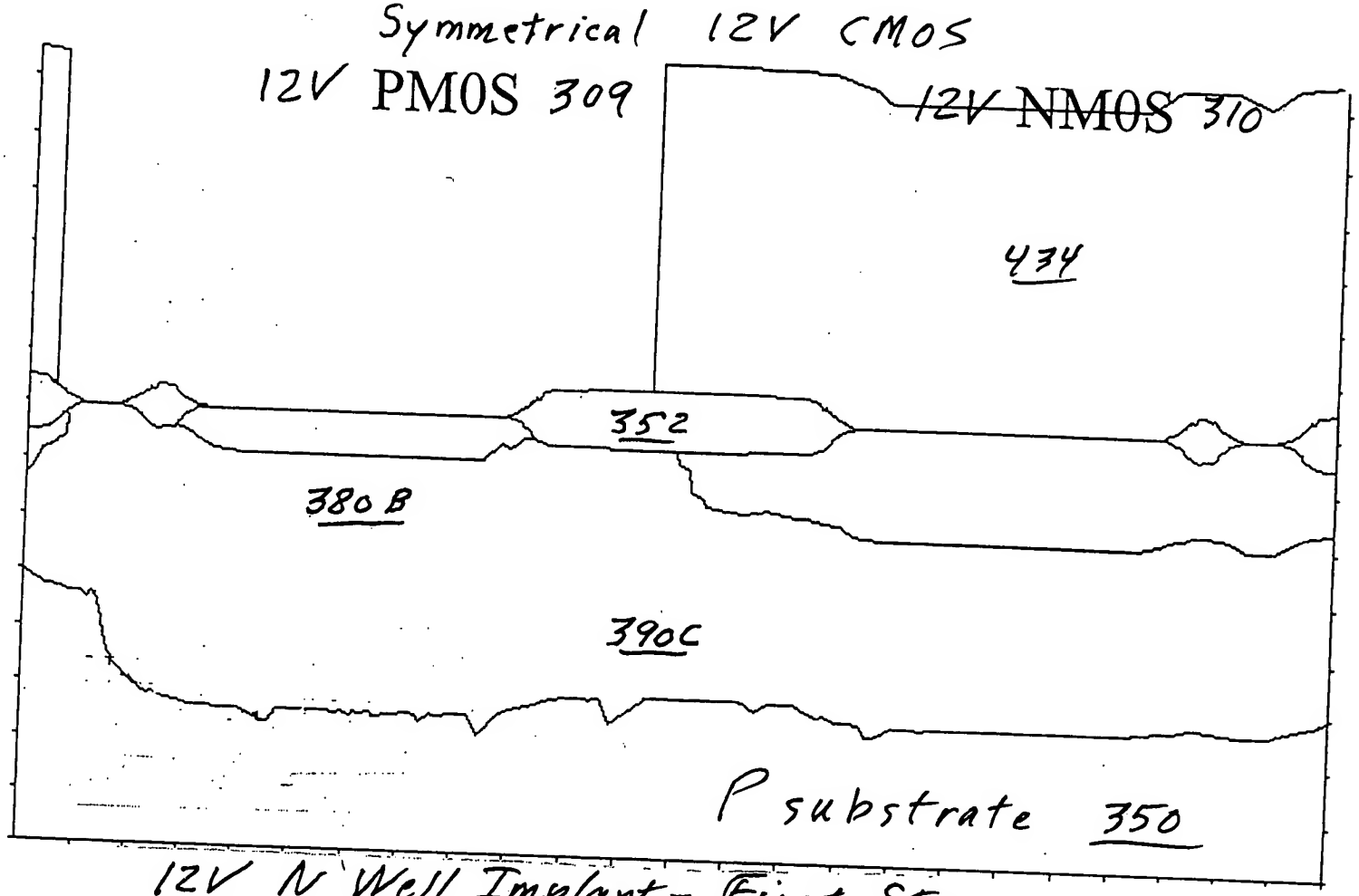
Fig. 36D

30 V Lateral Trench DMOS 308



N Drift Implant - Second Stage

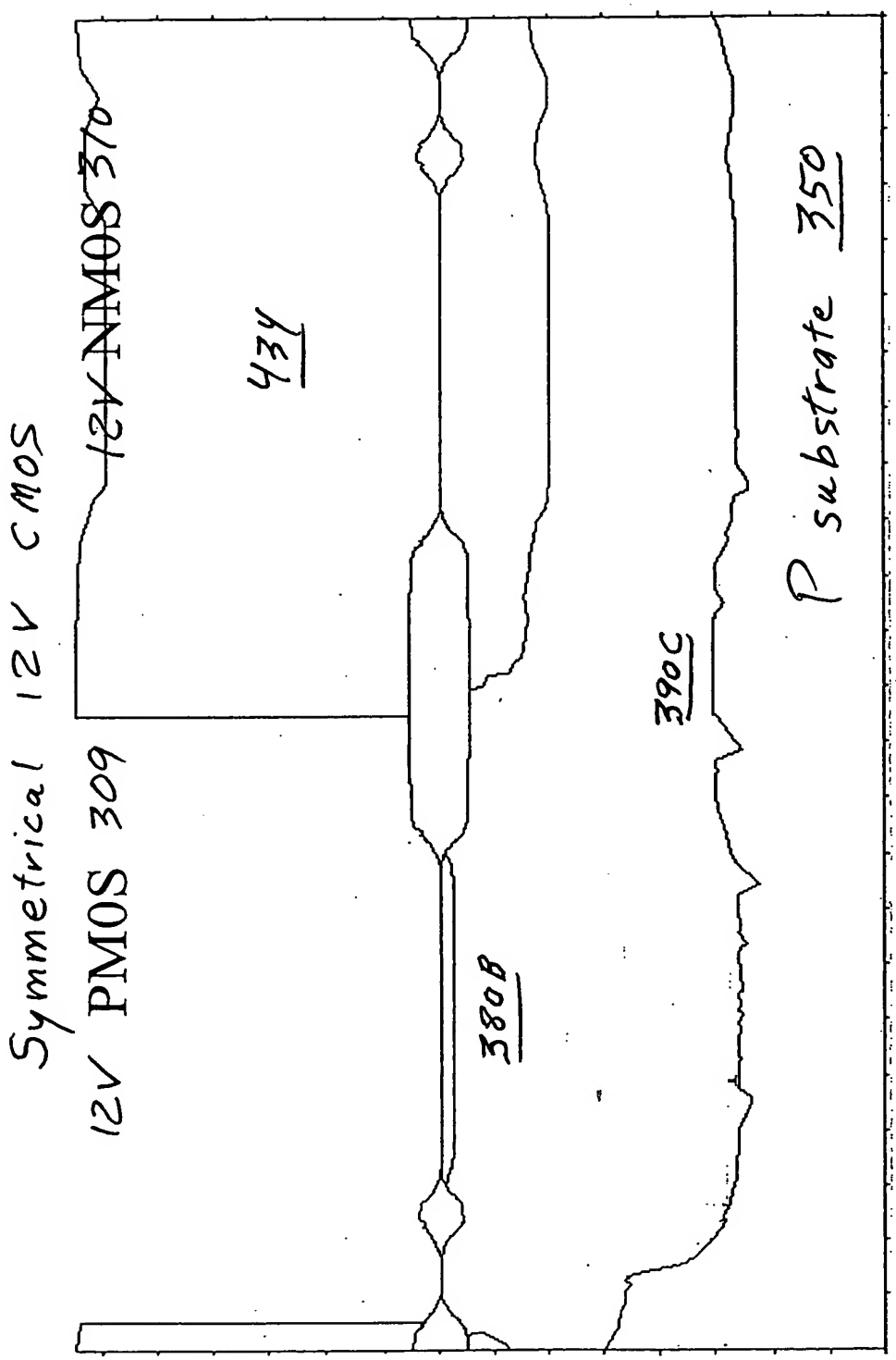
Fig. 37D



12V N Well Implant - First Stage

Fig. 38E

6/12/11


Symmetrical 12V CMOS
12V PMOS 309
12V NMOS 370
431
380B
390C
P substrate 350
12V N Well Implant - Second Stage

F.g. 39E

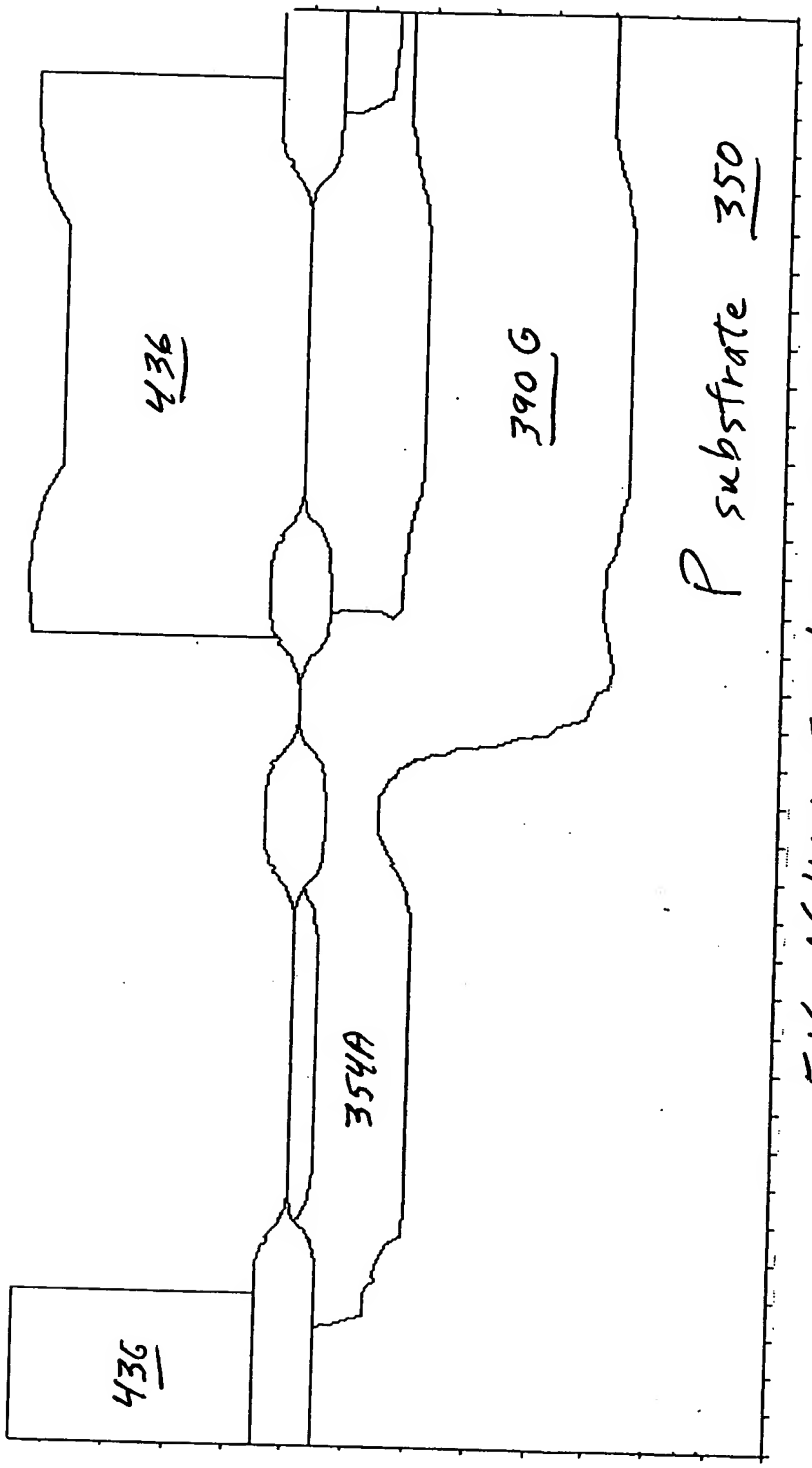
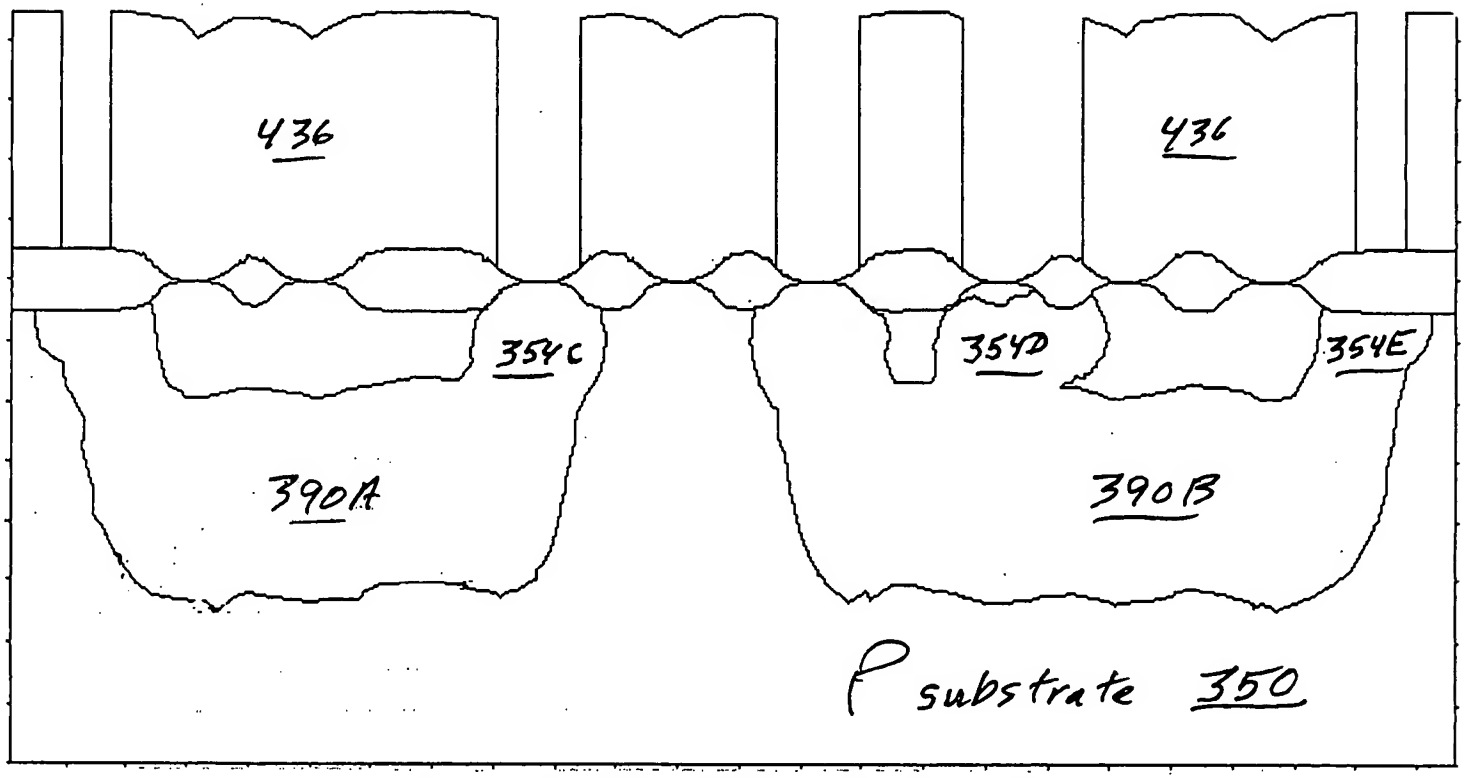

5V PMOS 301
5V NMOS 302
436
436
3540
390G
P substrate 350
5V N Well Implant - First Stage

Fig. 40M

High F_T Layout

5V NPN 305

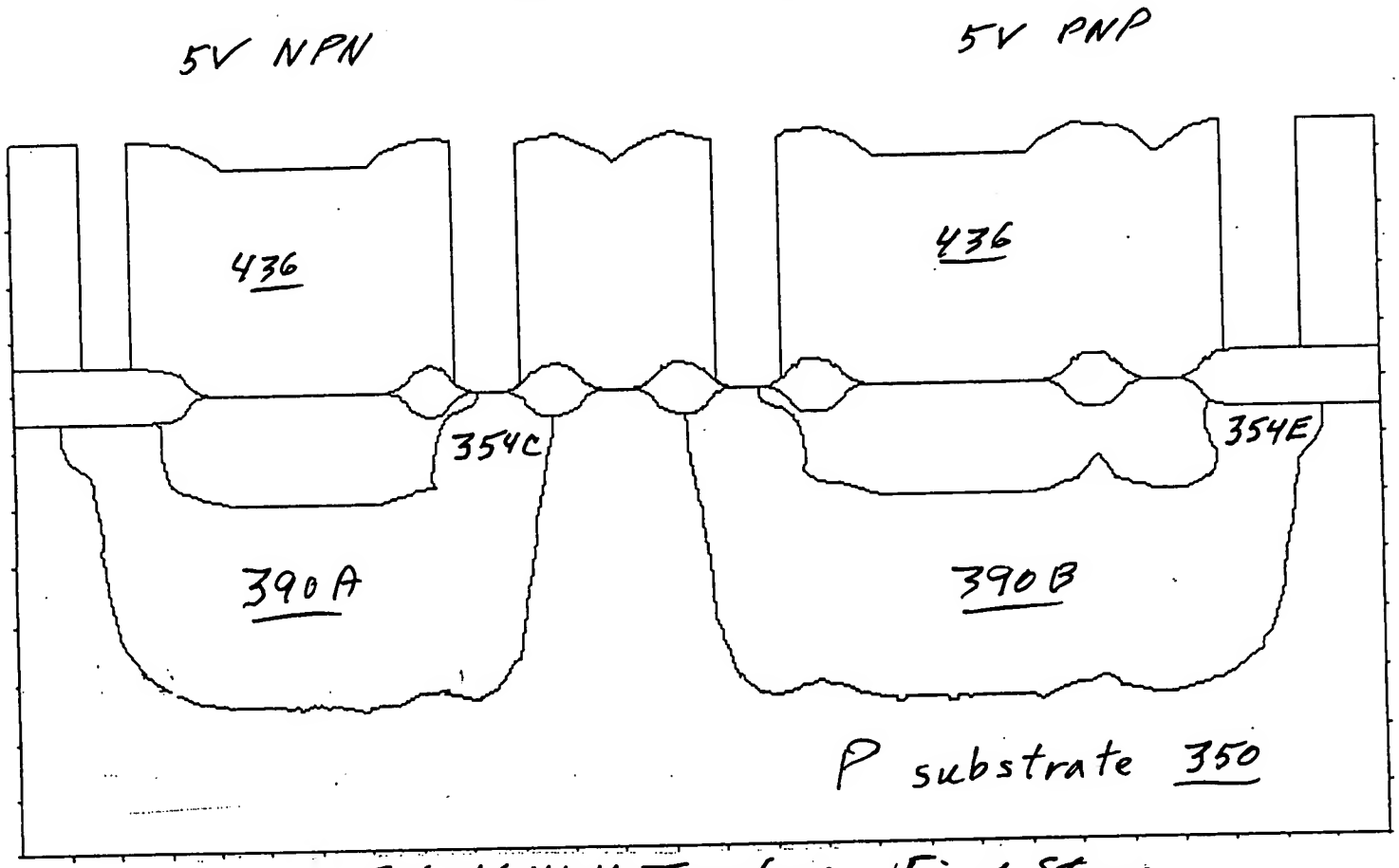
5V PNP 306



5V N Well Implant - First Stage

Fig. 40B

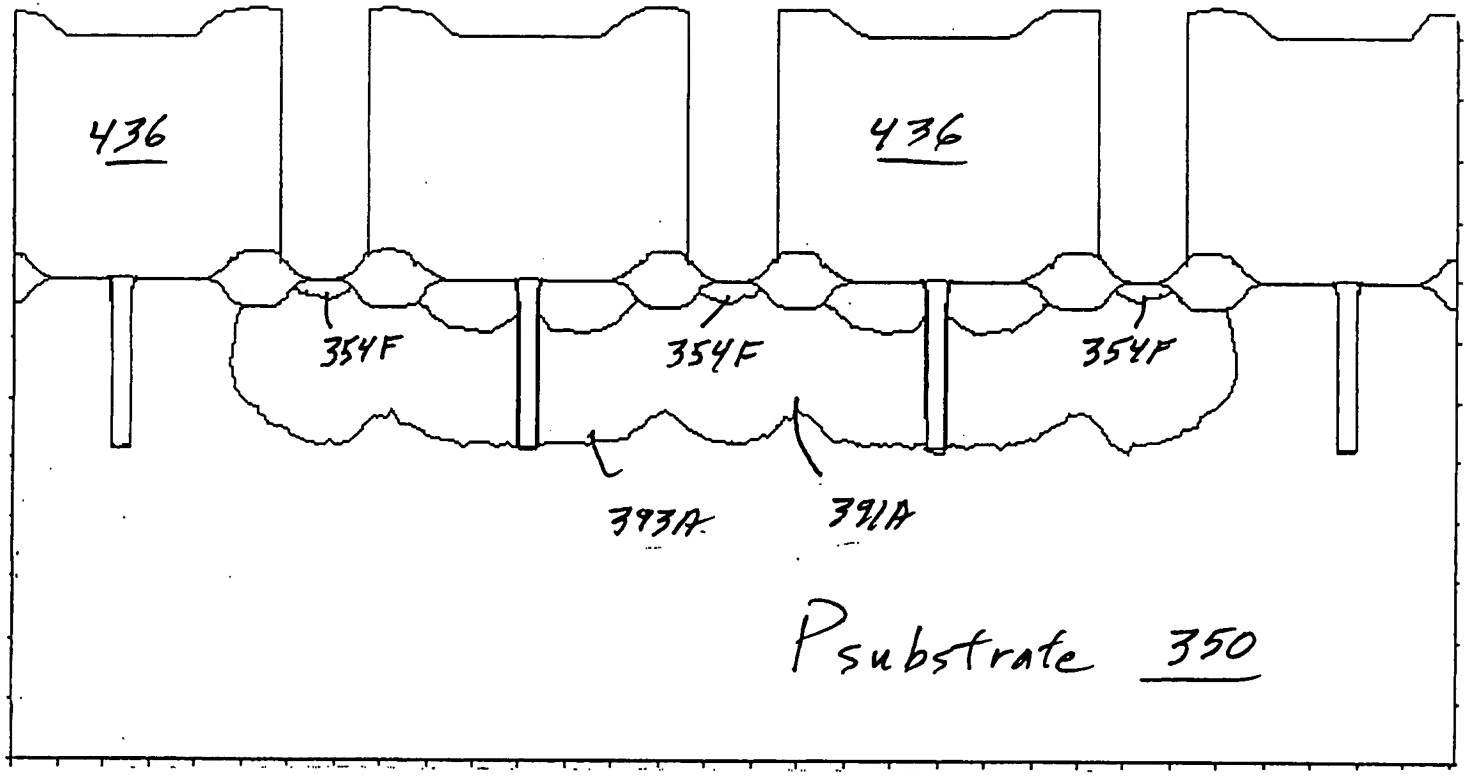
Conventional Layout



5V N Well Implant - First Stage

Fig. 40C

30V Lateral Trench DMOS 308

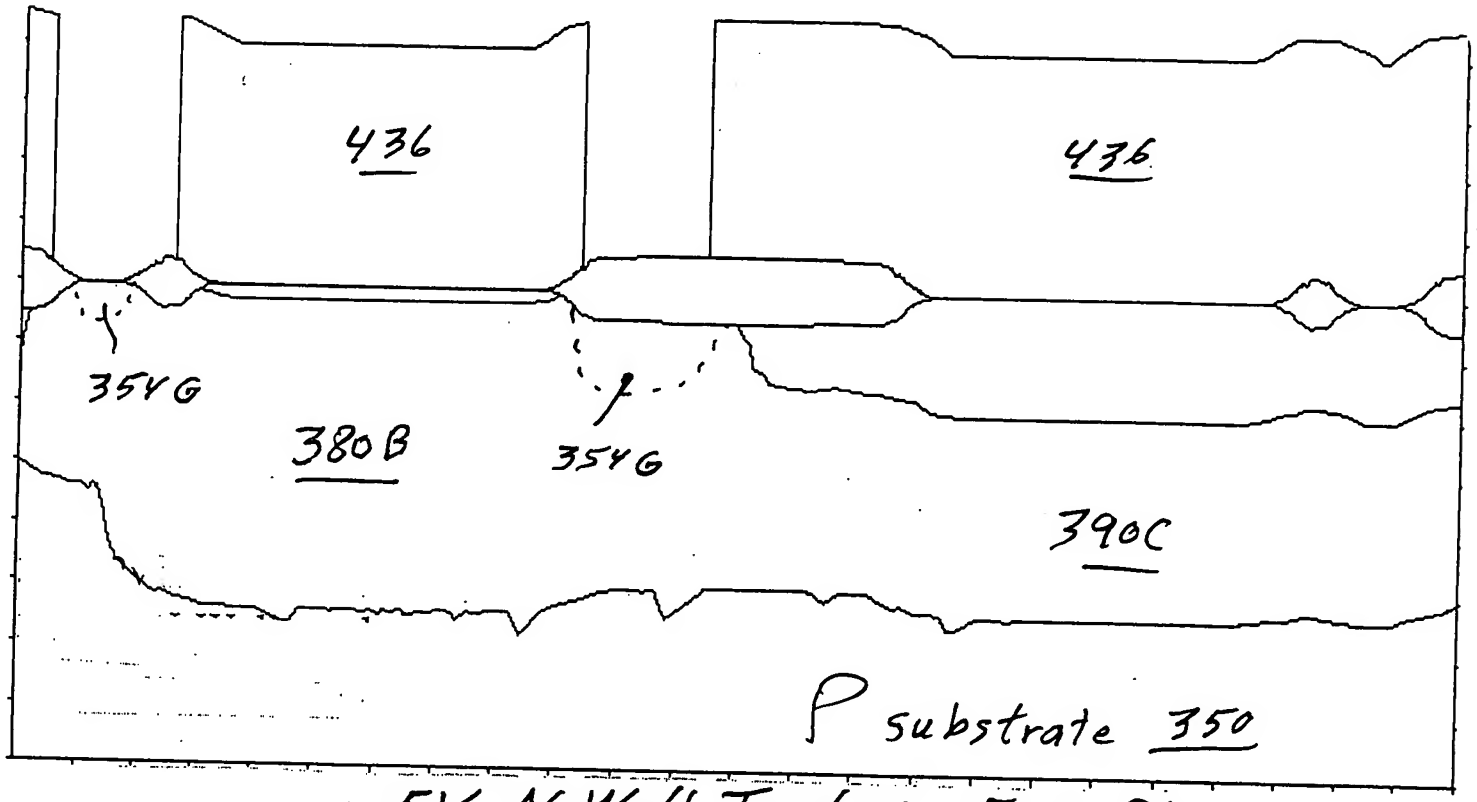


5V N Well Implant - First Stage

Fig. 40D

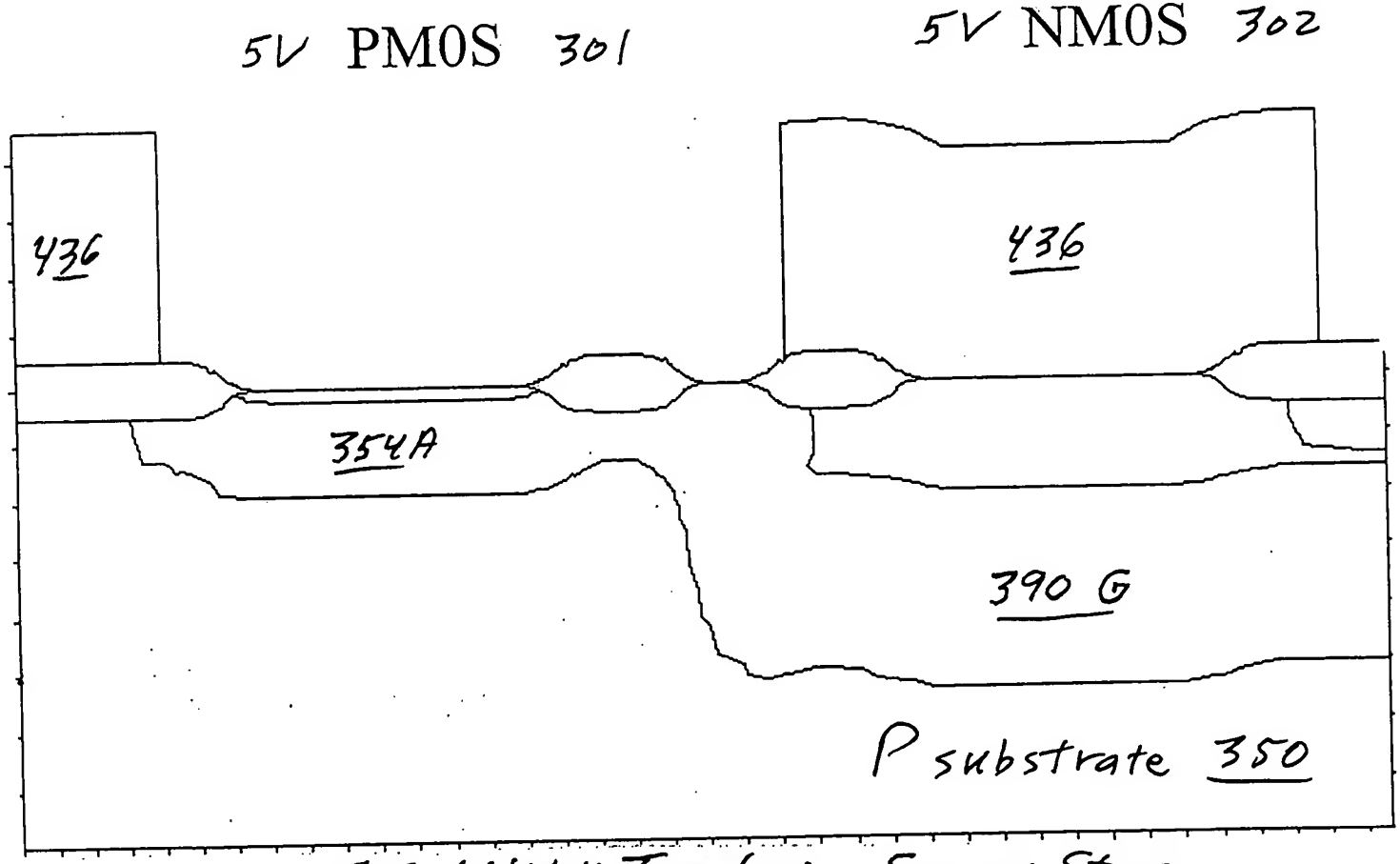
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



5V N Well Implant – First Stage

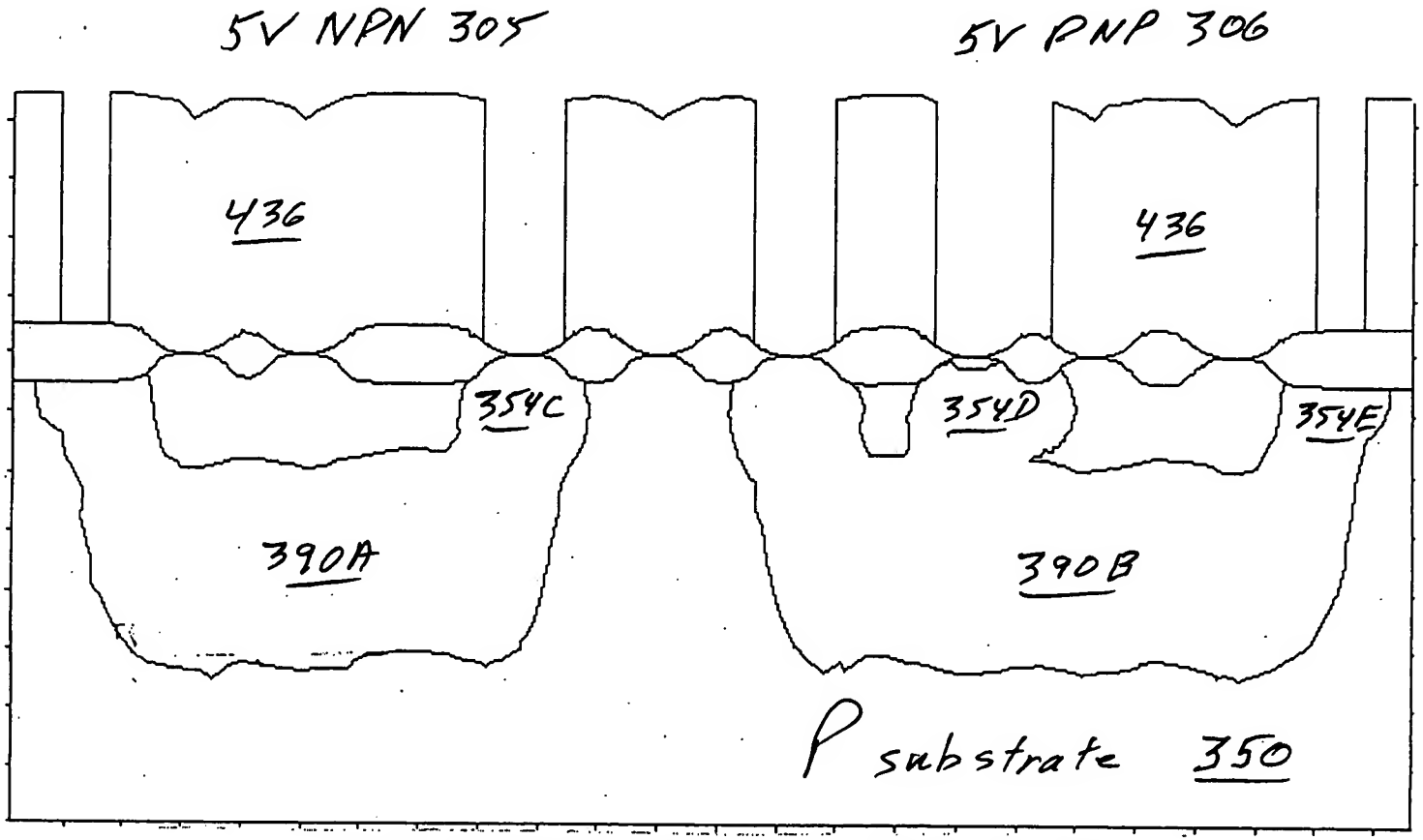
Fig 40E



5V N Well Implant - Second Stage

Fig. 41A

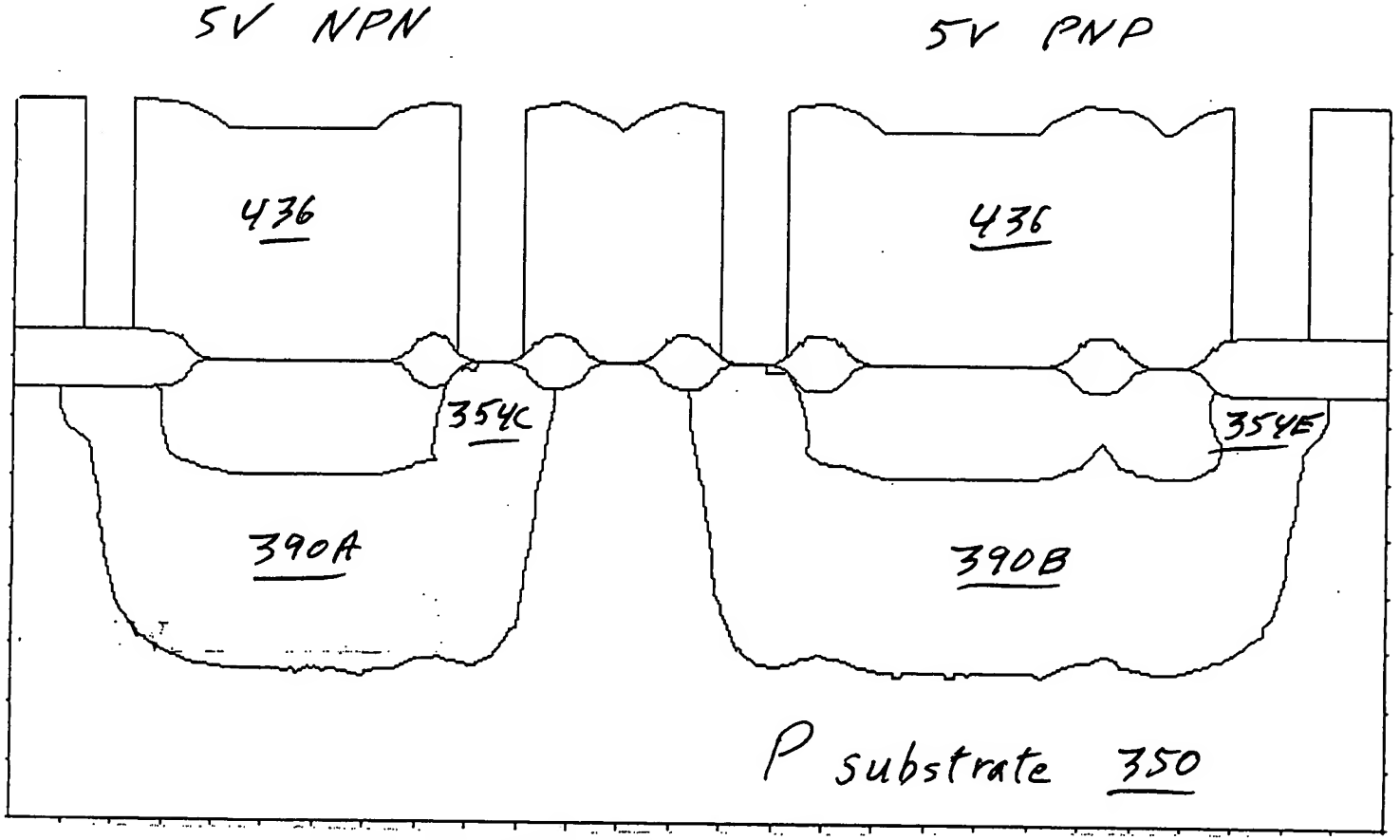
High F_T Layout



5V N Well Implant - Second Stage

Fig. 41B

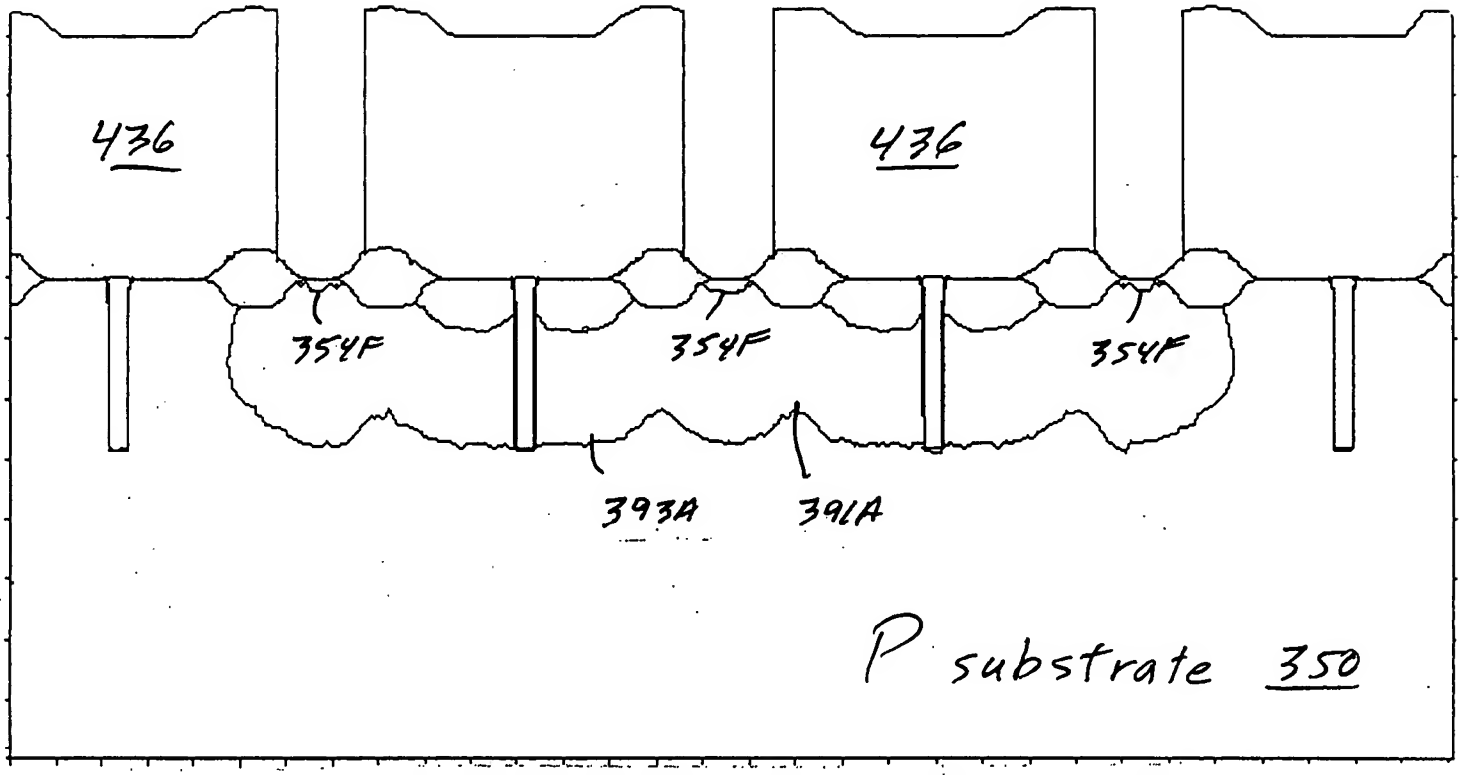
Conventional Layout



5V N Well Implant - Second Stage

Fig. 41C

30V Lateral Trench DMOS 308

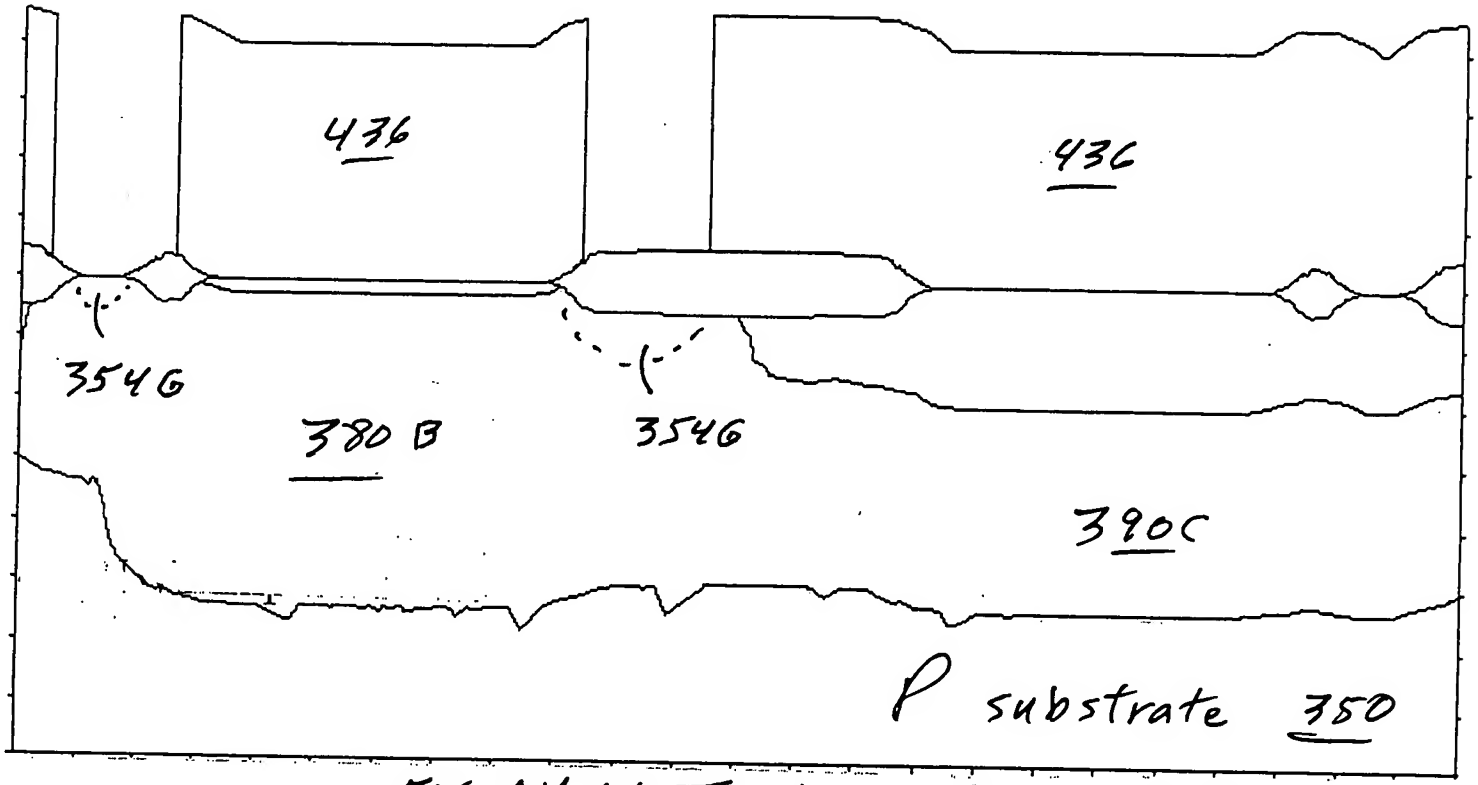


5V N Well Implant - Second Stage

Fig. 41D

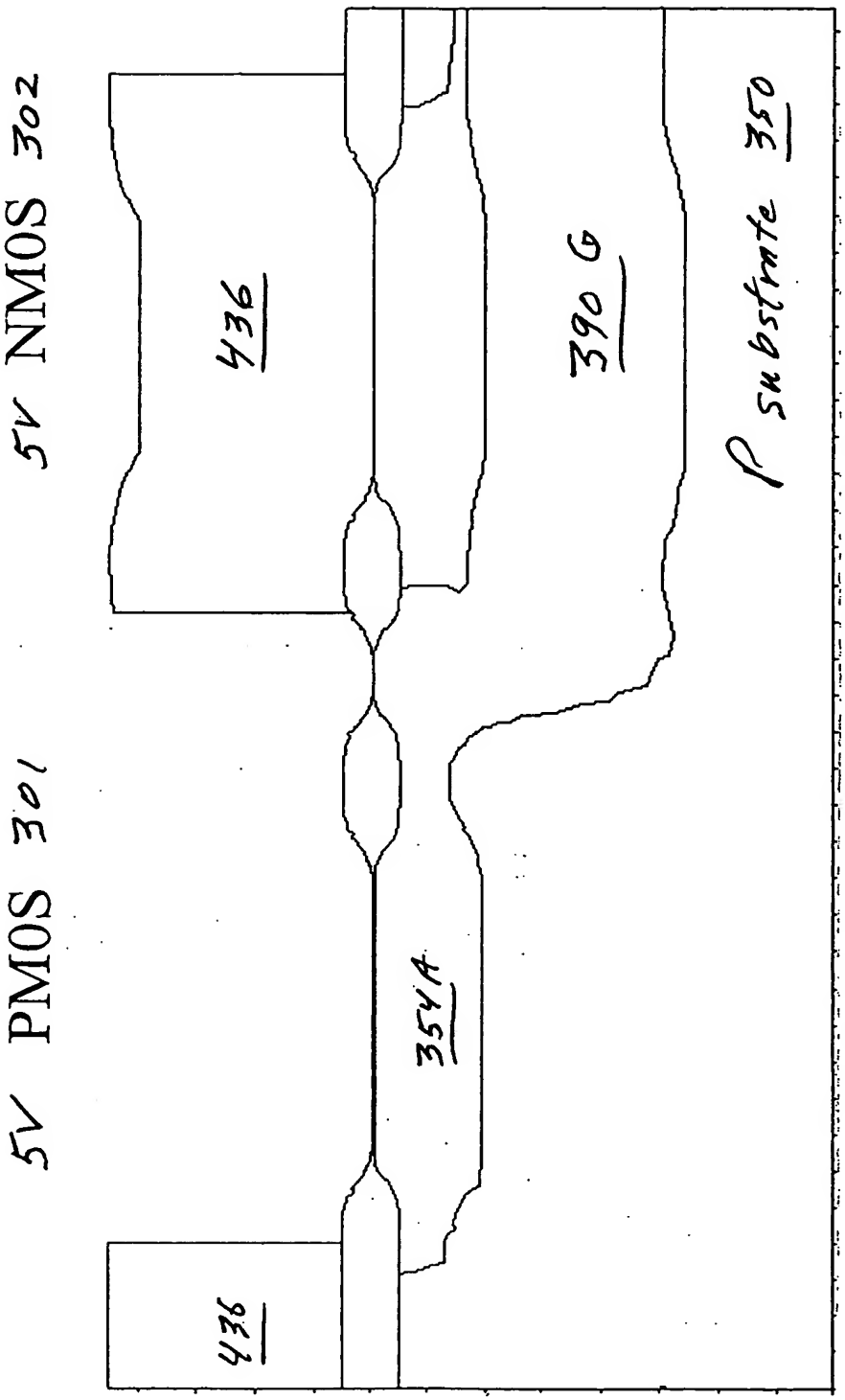
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



5V NWell Implant - Second Stage

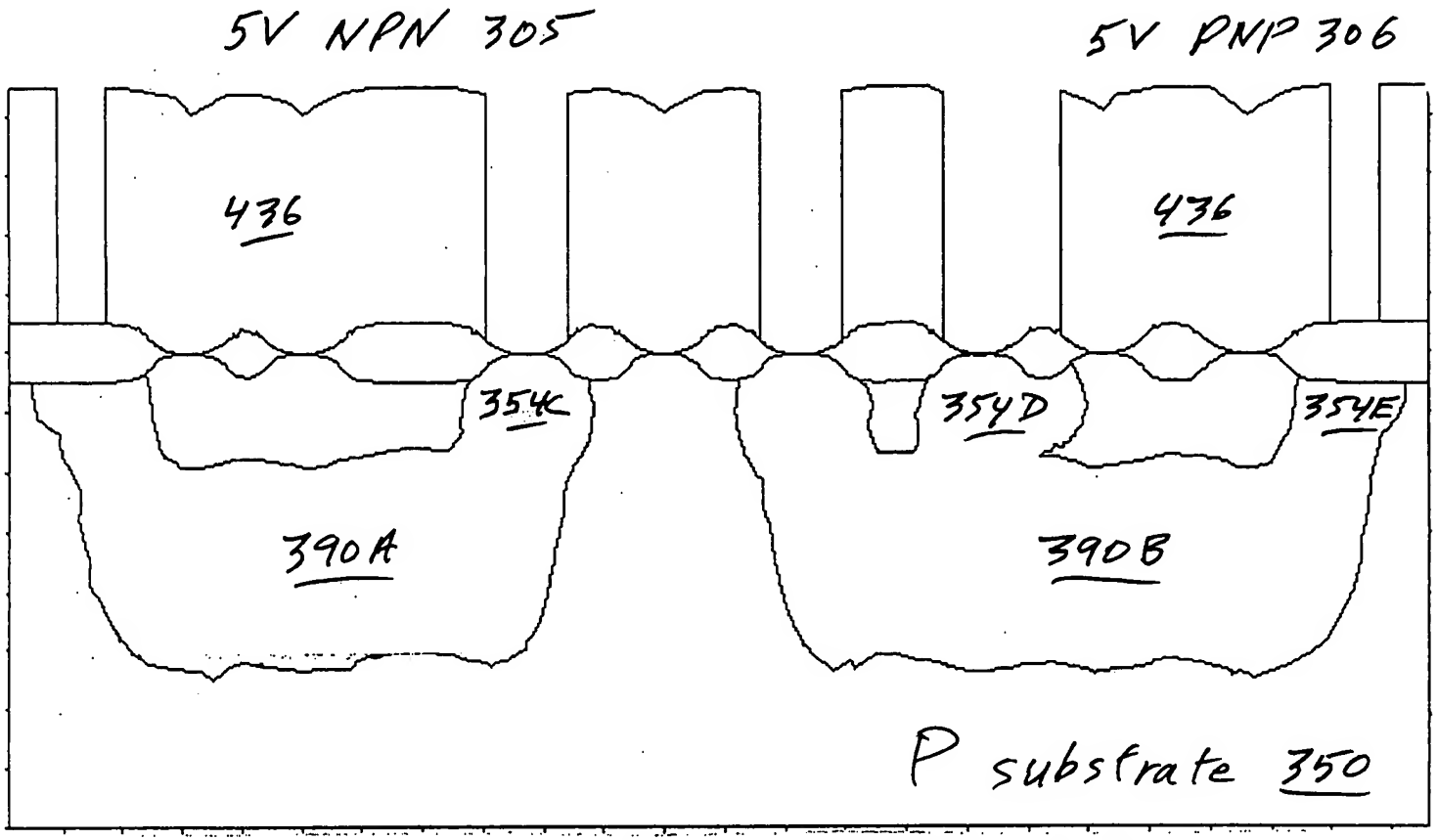
Fig. 41E



5V N Well Implant - Third Stage

Fig. 42A

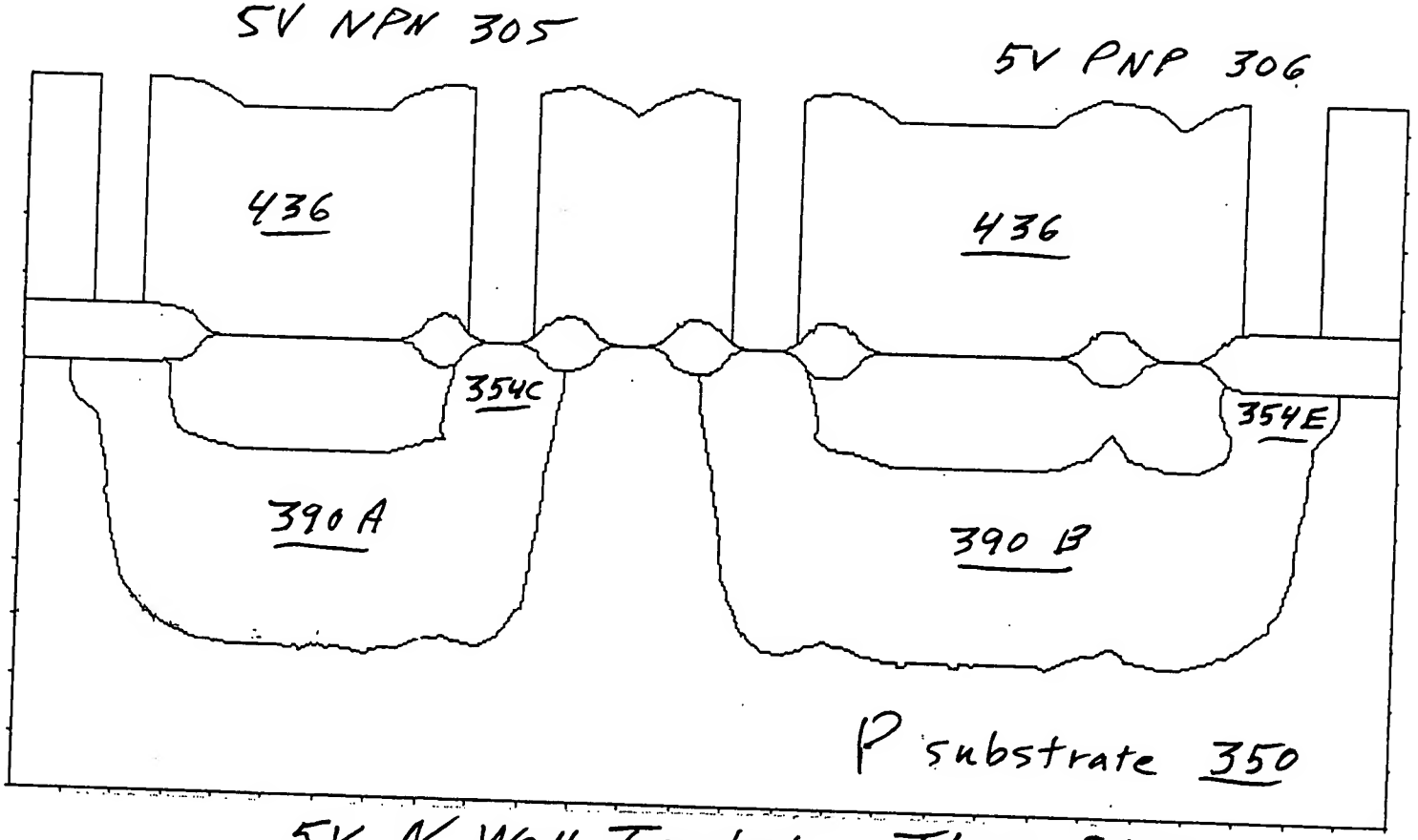
High F_T Layout



5V N Well Implant - Third Stage

Fig. 42B

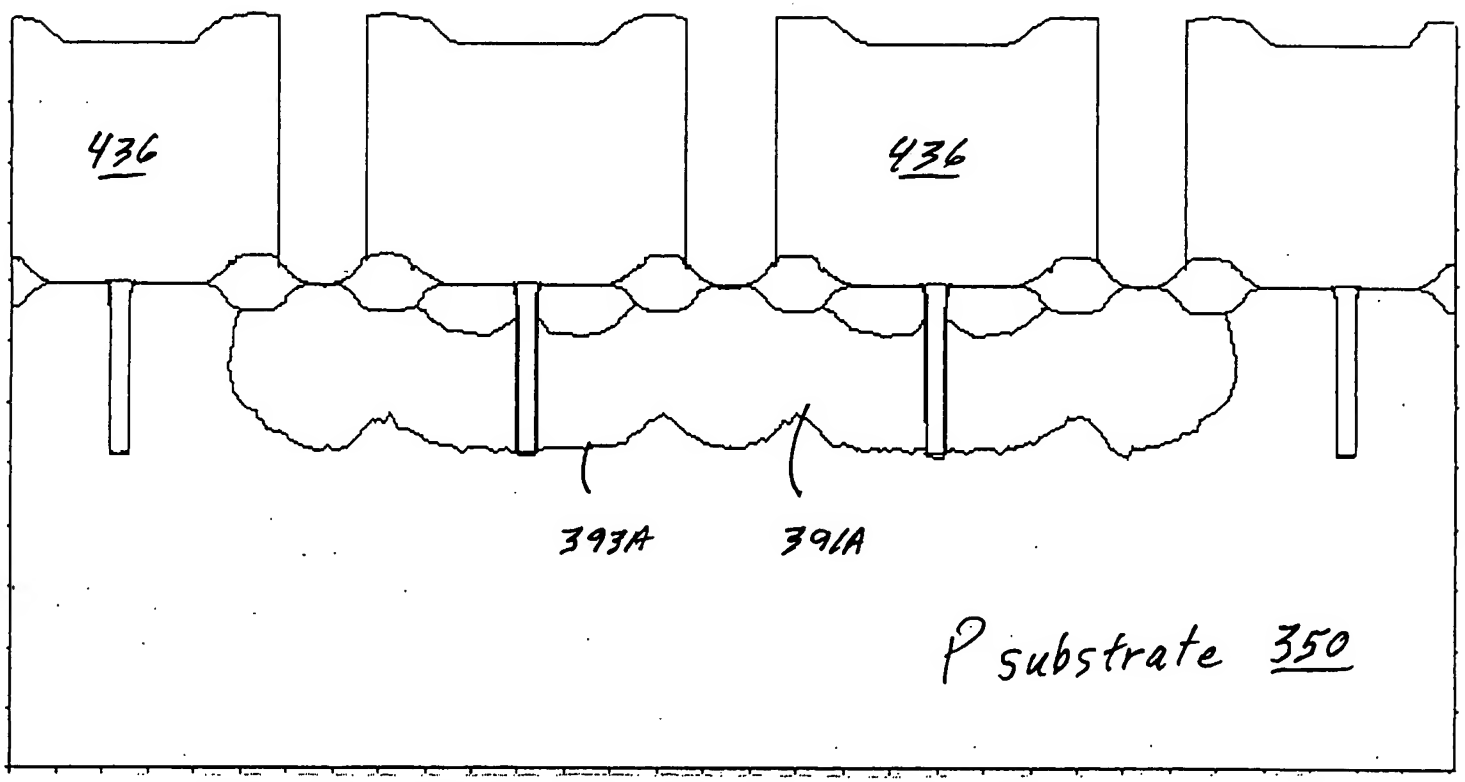
Conventional Layout



5V N Well Implant – Third Stage

Fig. 42C

30V Lateral Trench DMOS 308

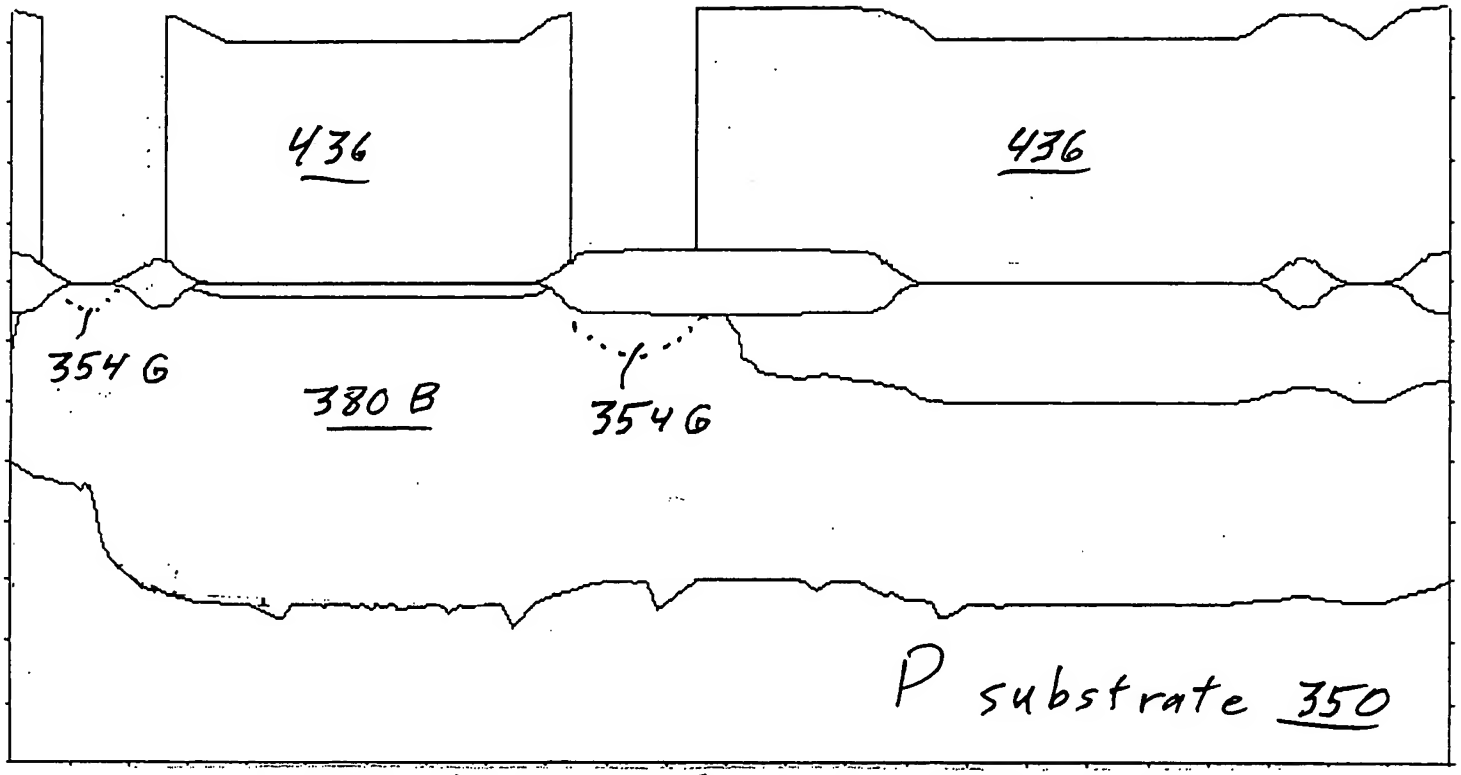


5V N Well Implant - Third Stage

Fig. 42D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



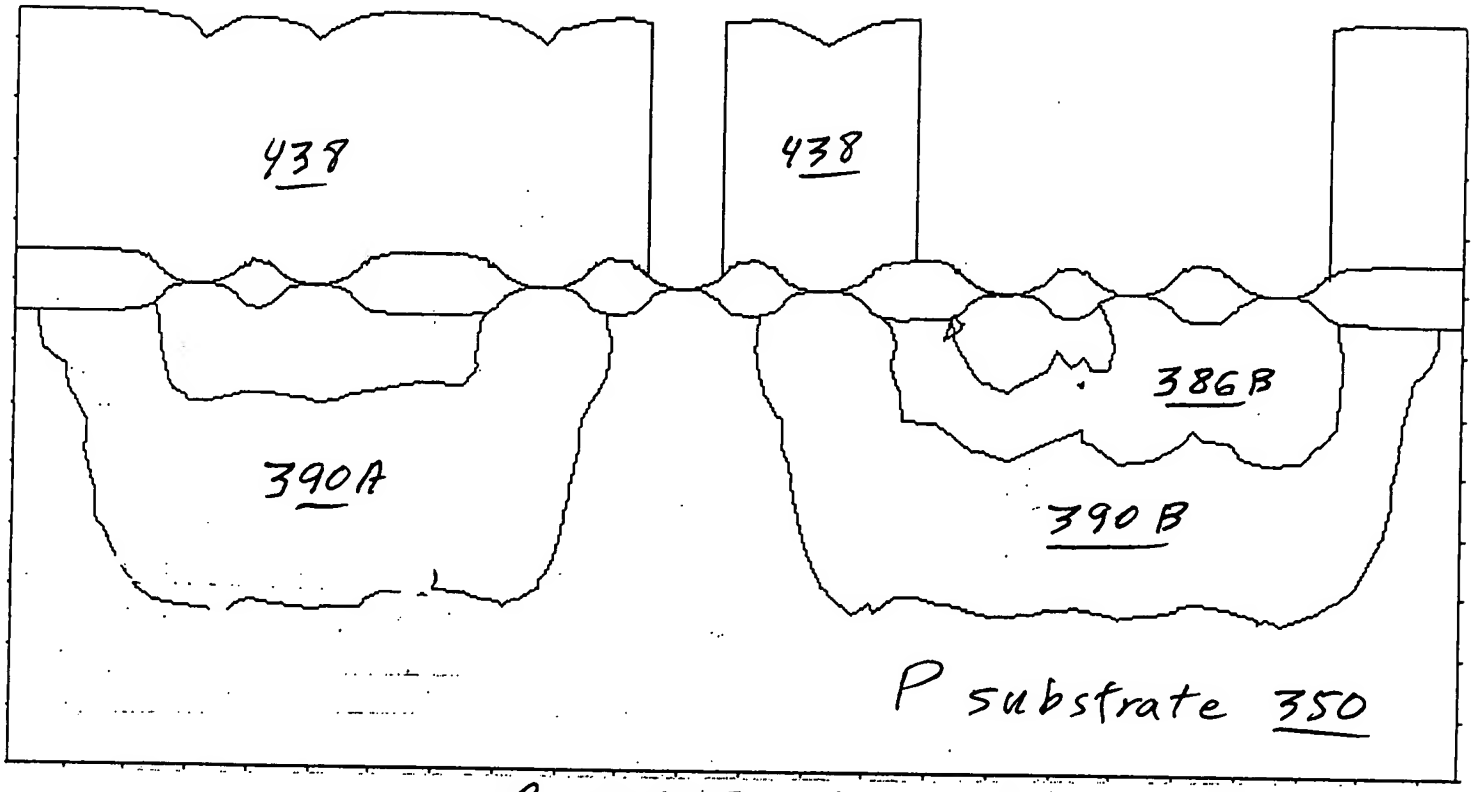
5V N Well Implant – Third Stage

Fig. 42E

High F_T Layout

5V NPN 305

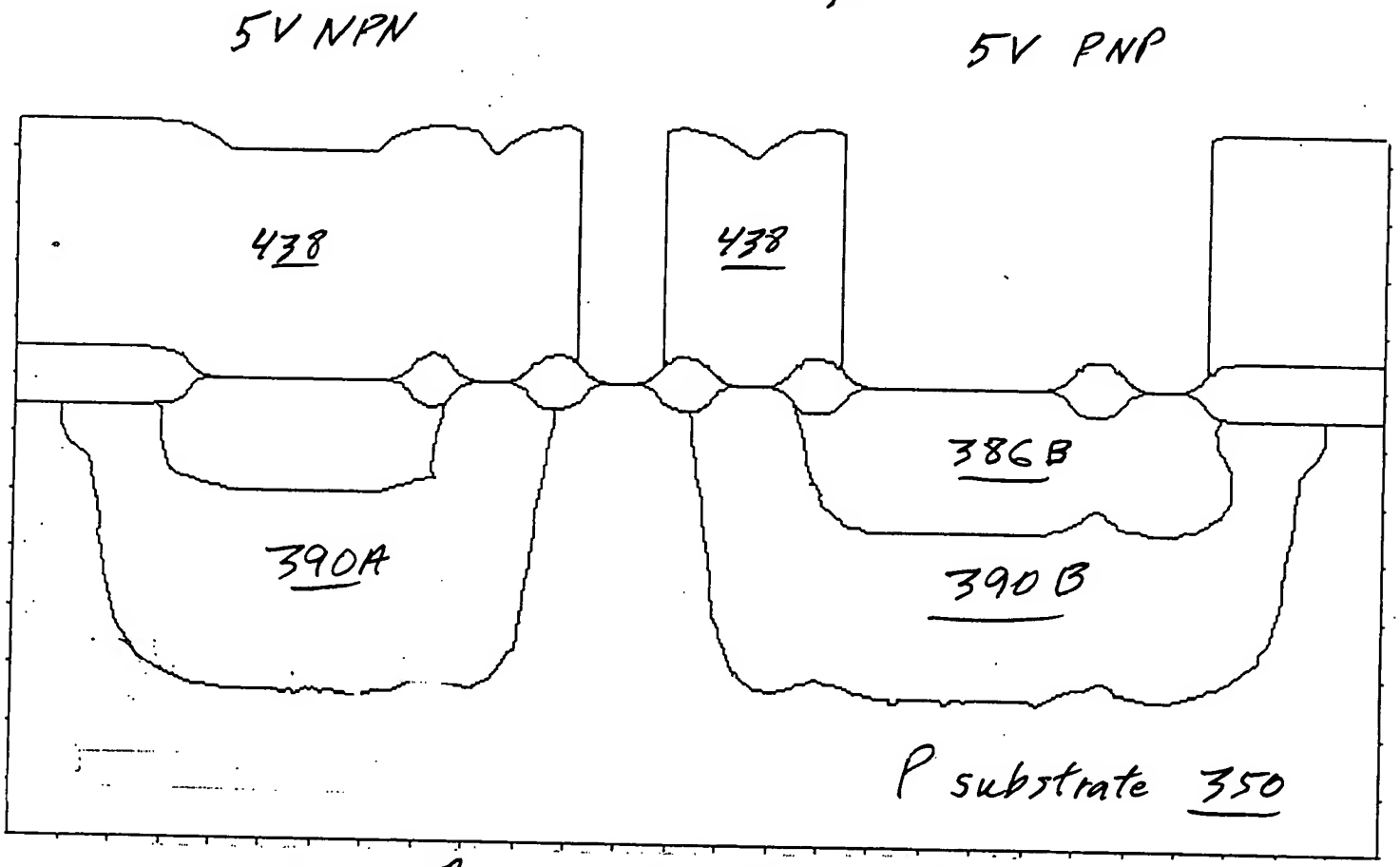
5V PNP 306



12V P Well Implant - First Stage

Fig. 43B

Conventional Layout

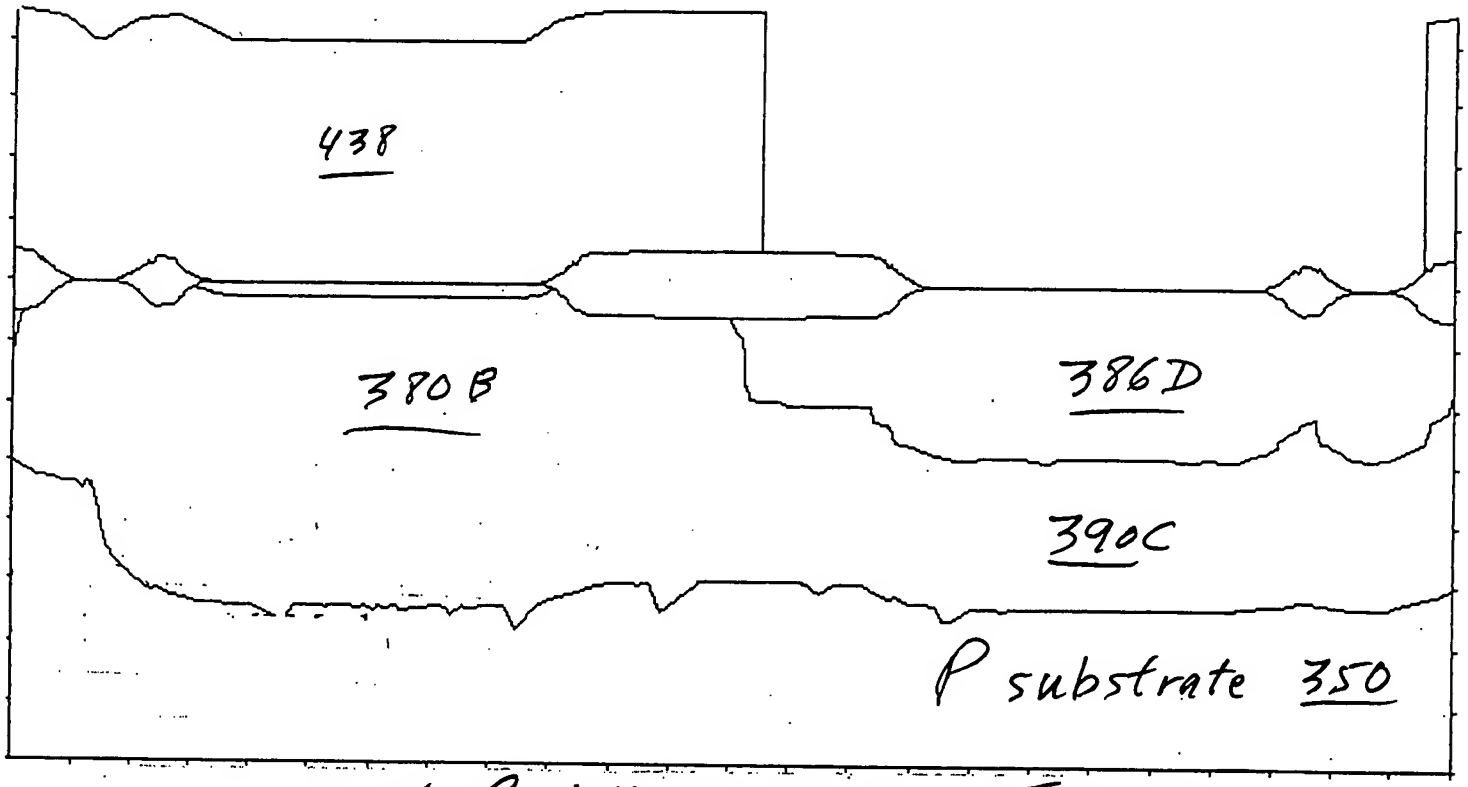


12V P Well Implant – First Stage

Fig. 43C

Symmetrical 12V CMOS

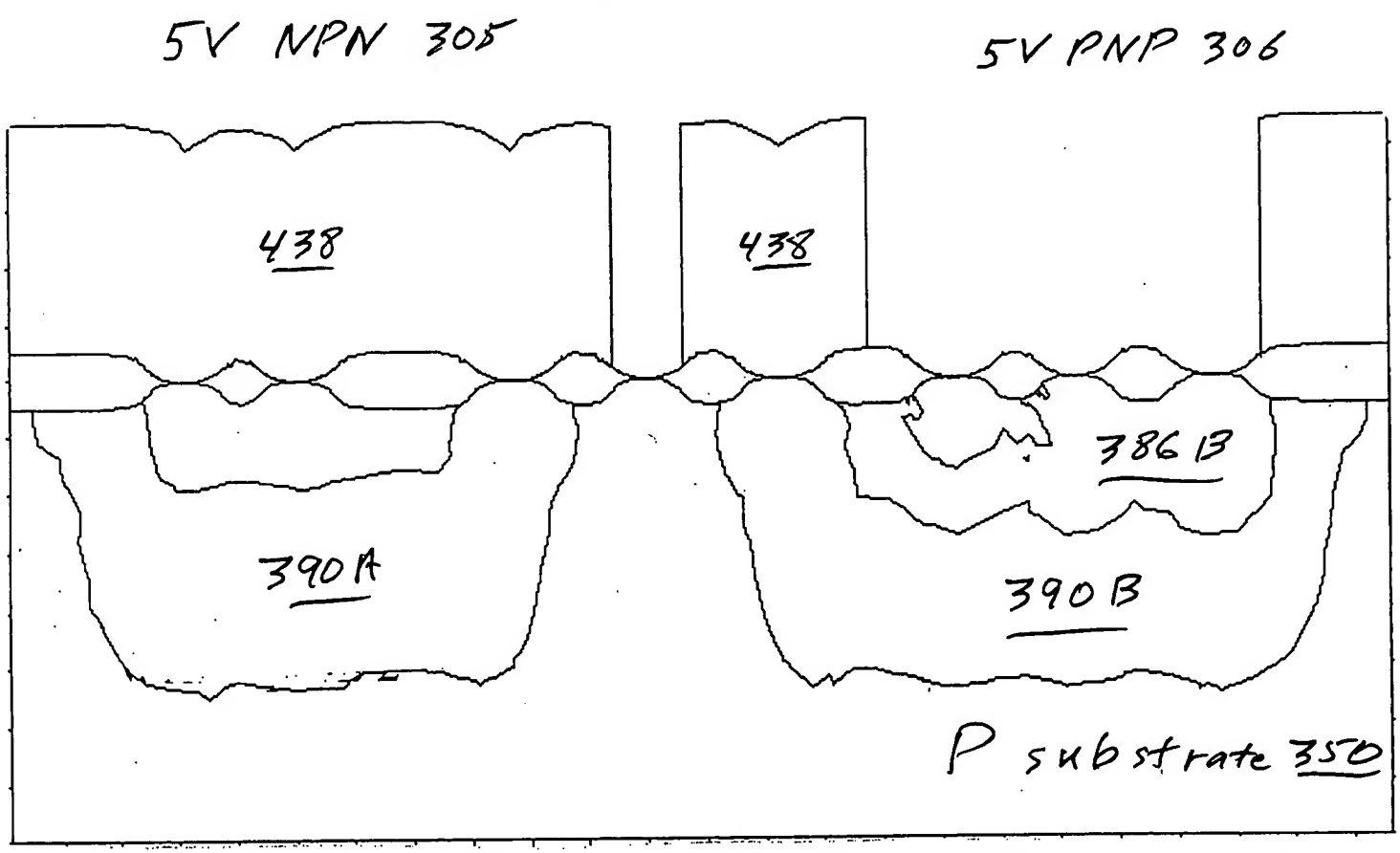
12V PMOS 309 12V NMOS 310



12V PWell Implant - First Stage

Fig 43E

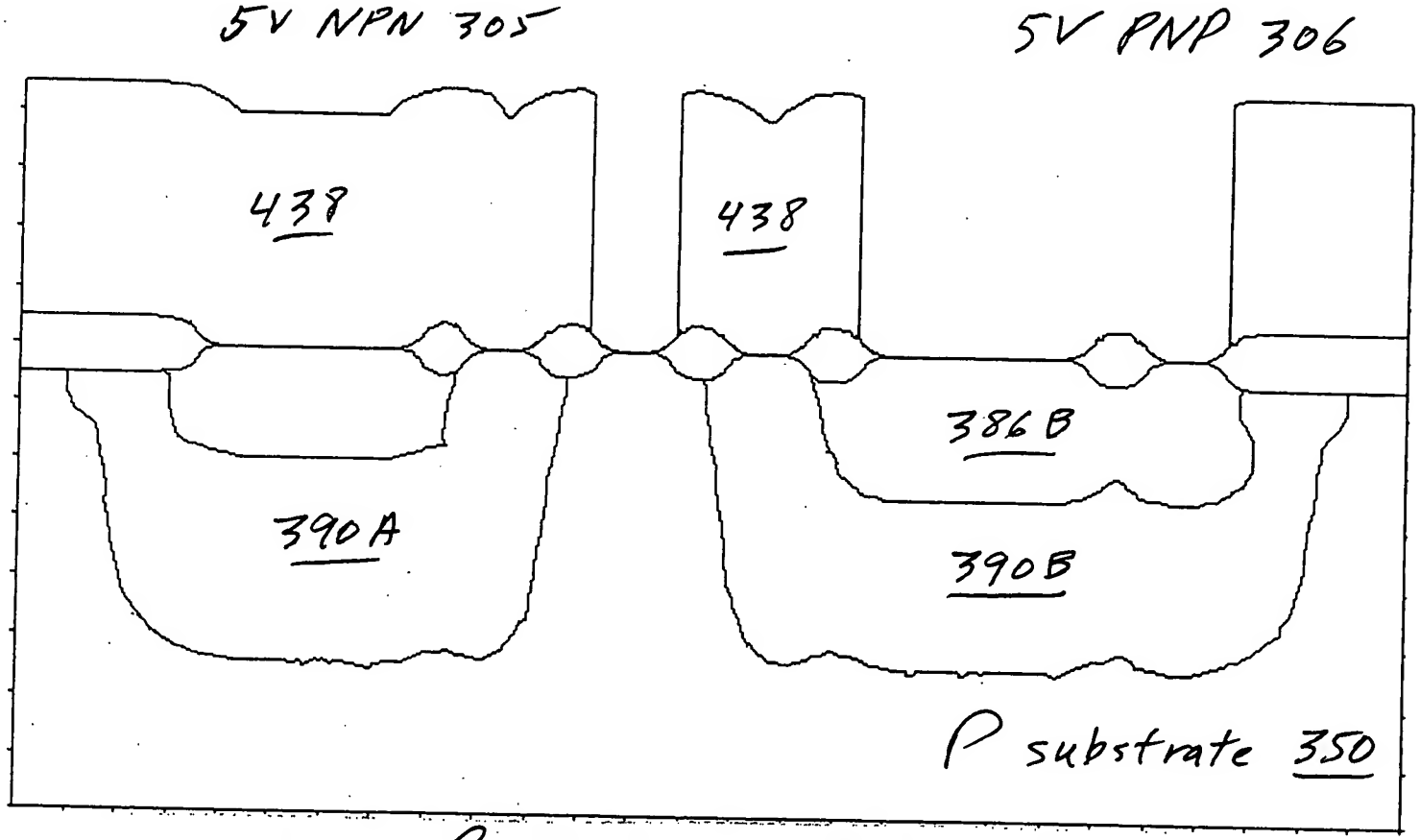
High F_T Layout



12V P Well Implant - Second Stage

Fig. 44B

Conventional Layout

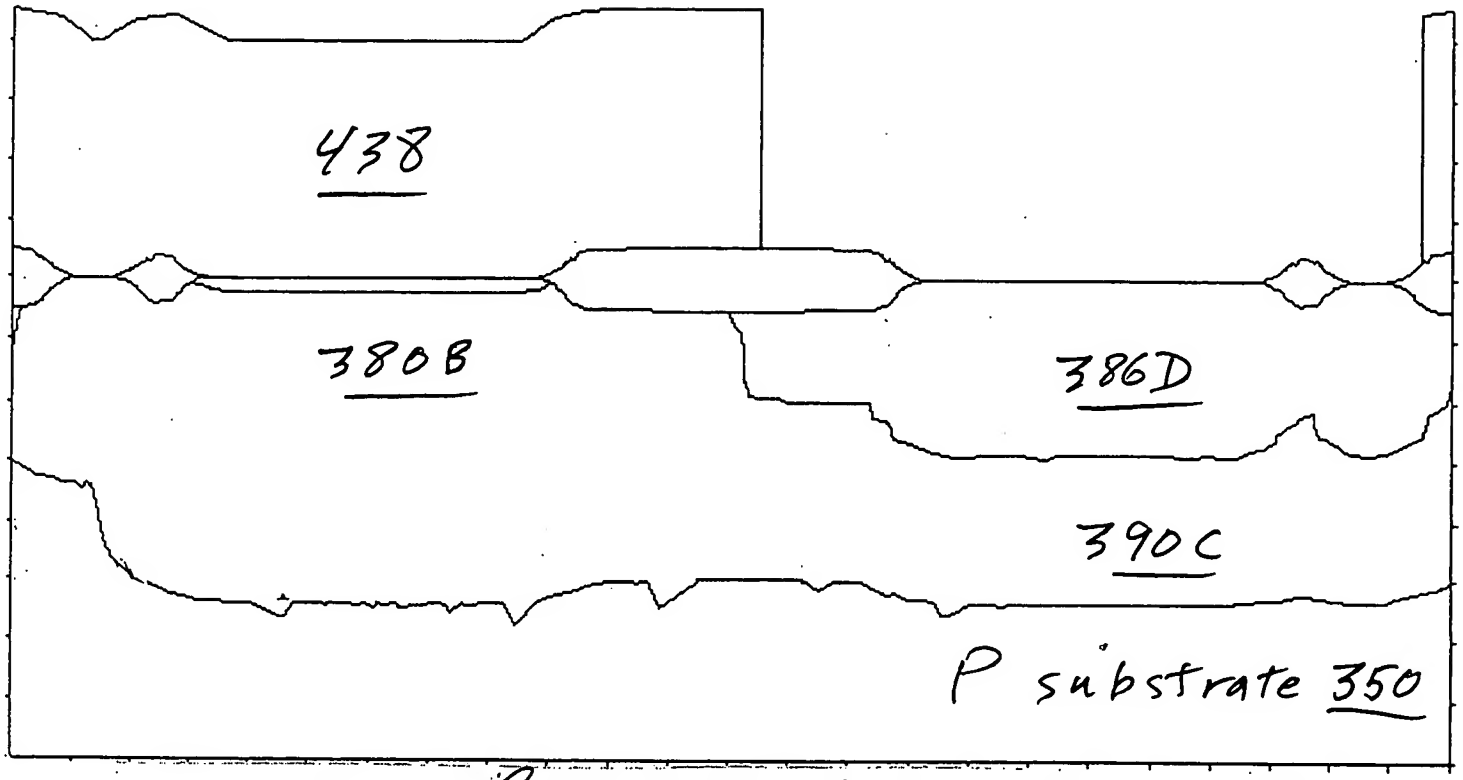


12V P Well Implant - Second Stage

Fig 44C

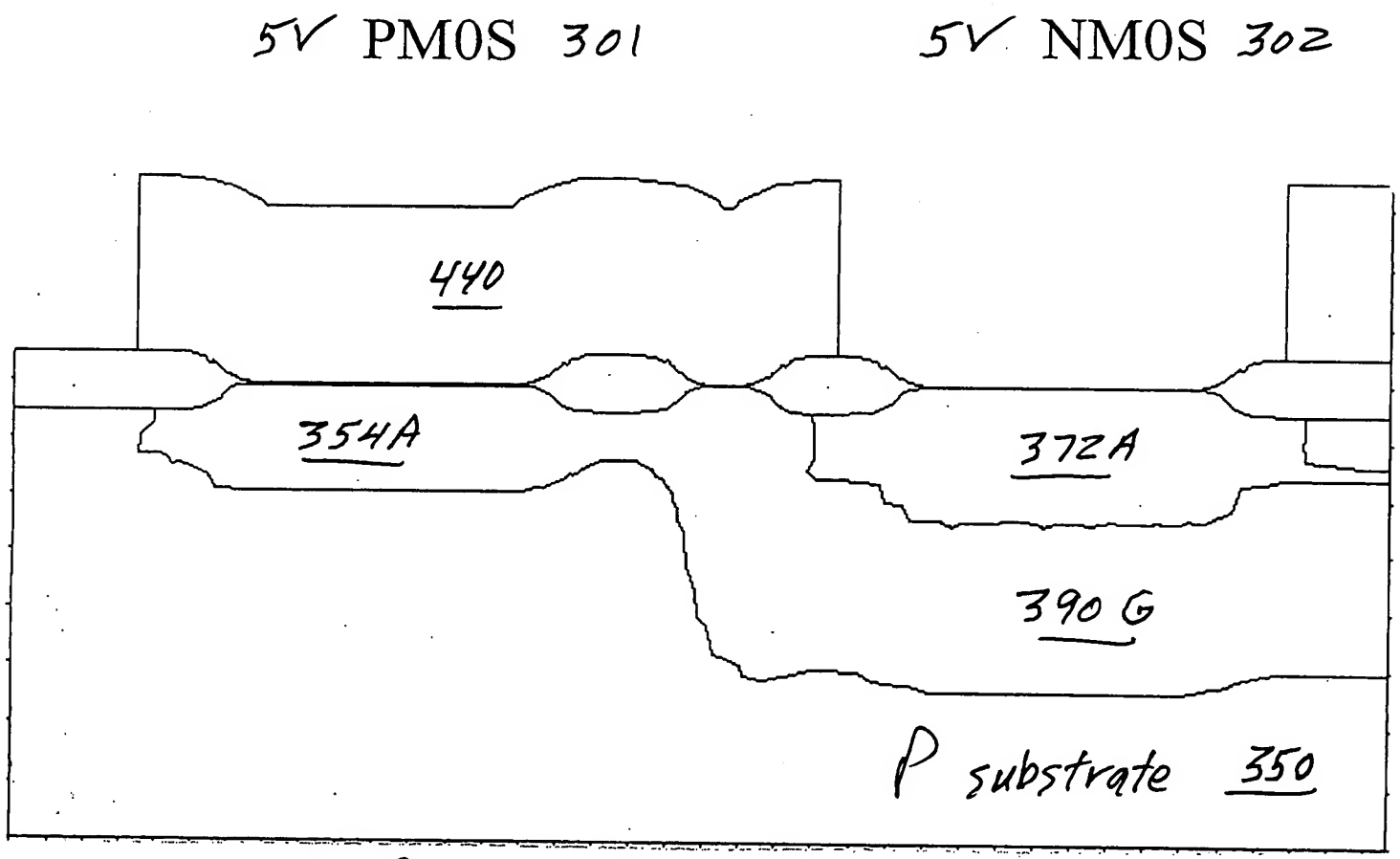
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



12 V P Well Implant – Second Stage

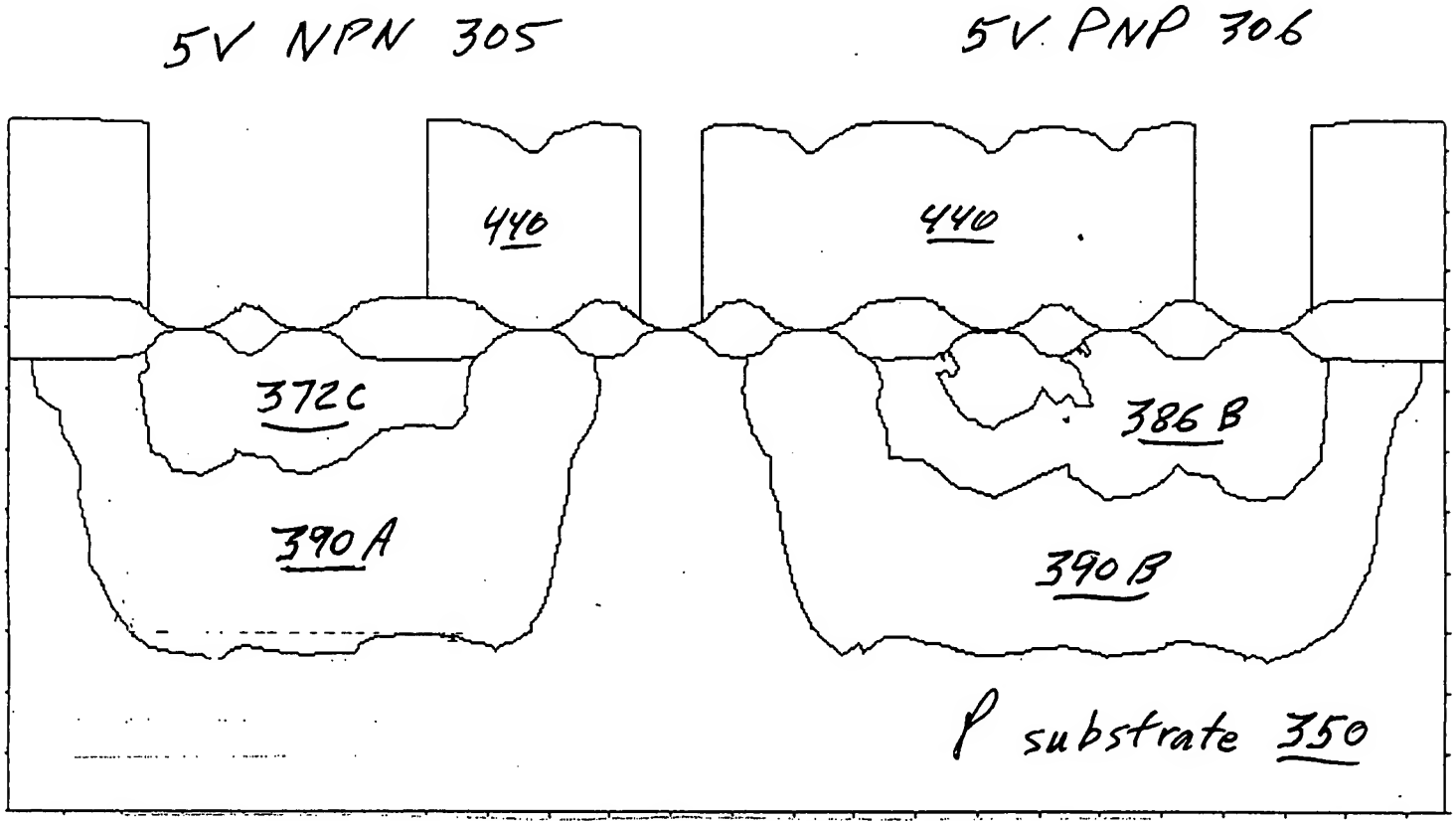
Fig. 44E



5 V P Well Implant - First Stage

Fig. 45A

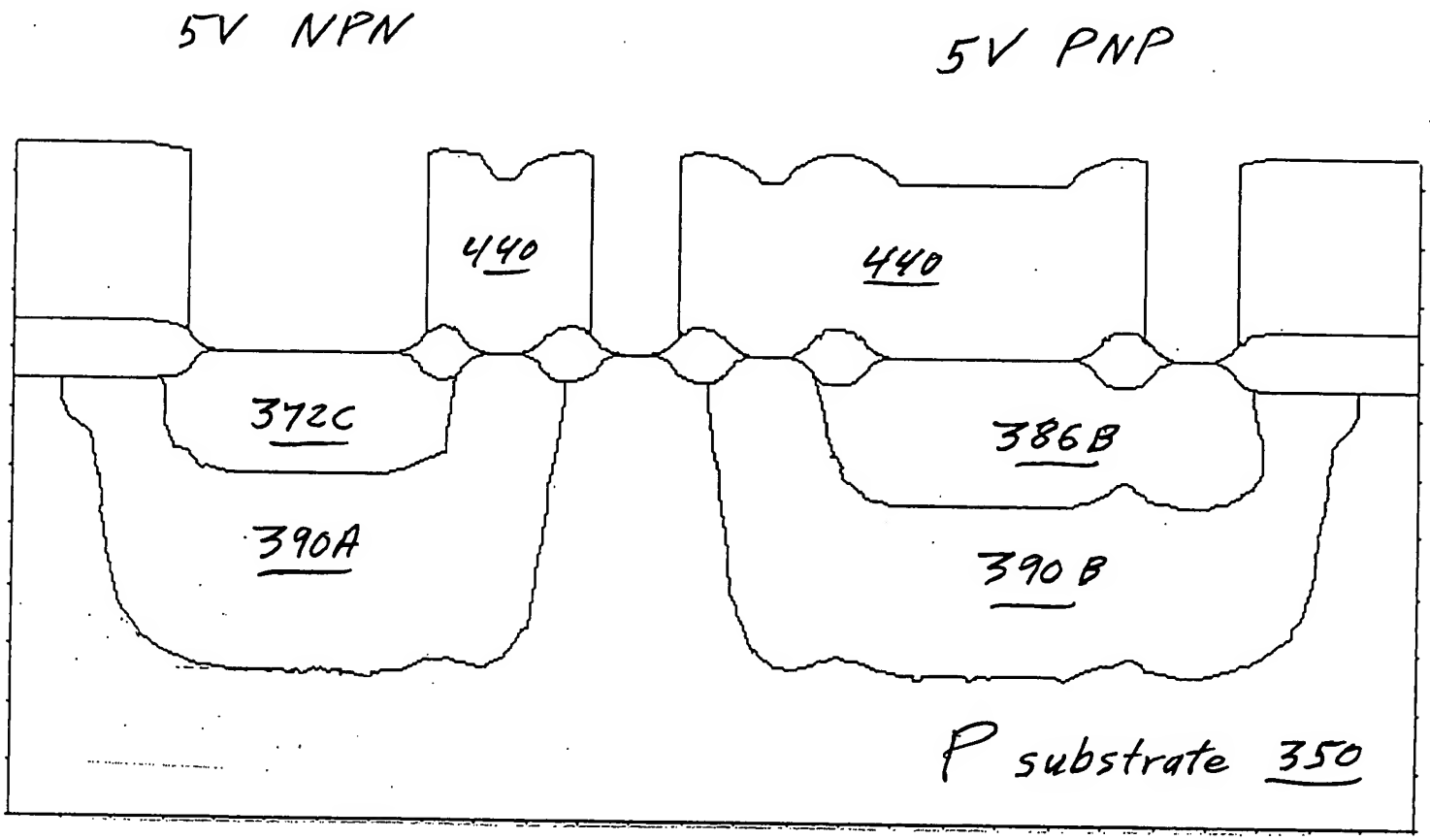
High F_T Layout



5V P Well Implant – First Stage

Fig. 45B

Conventional Layout

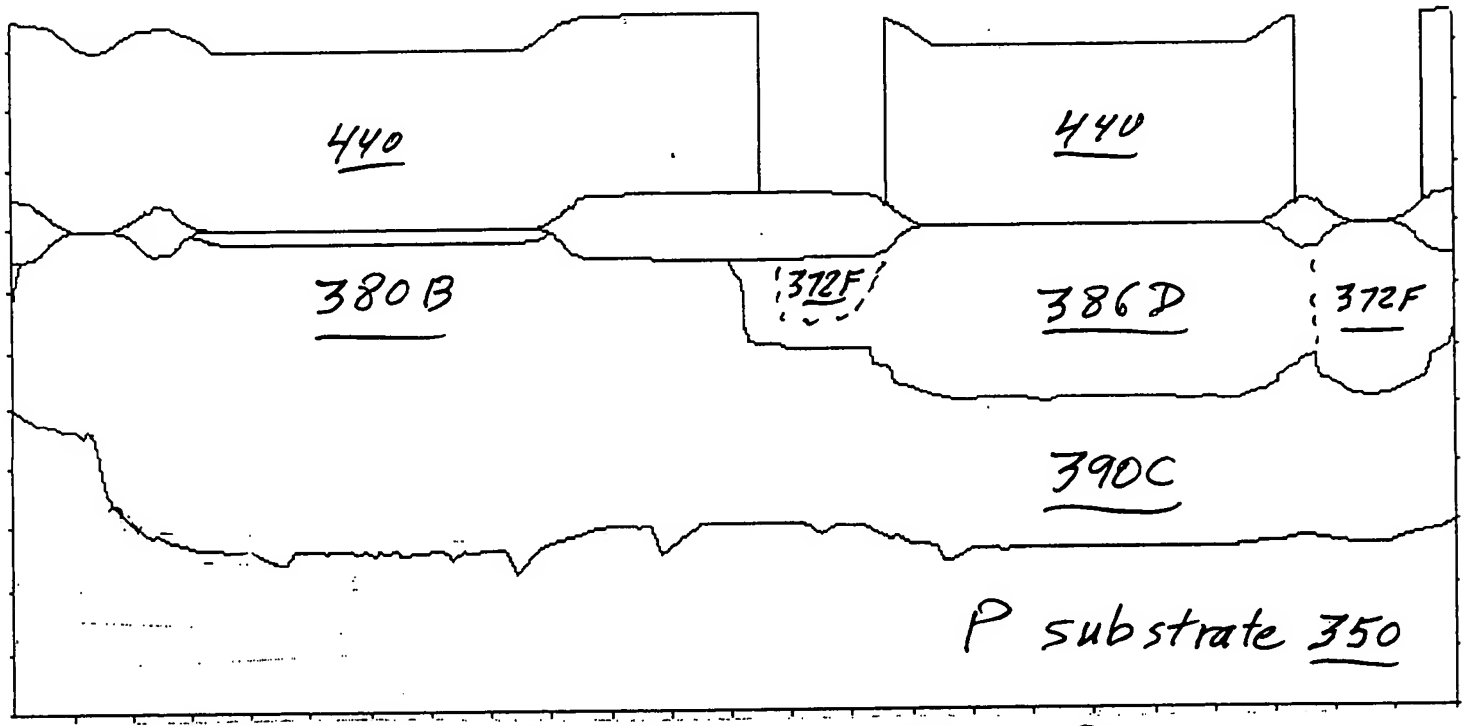


5V P Well Implant - First Stage

Fig. 45C

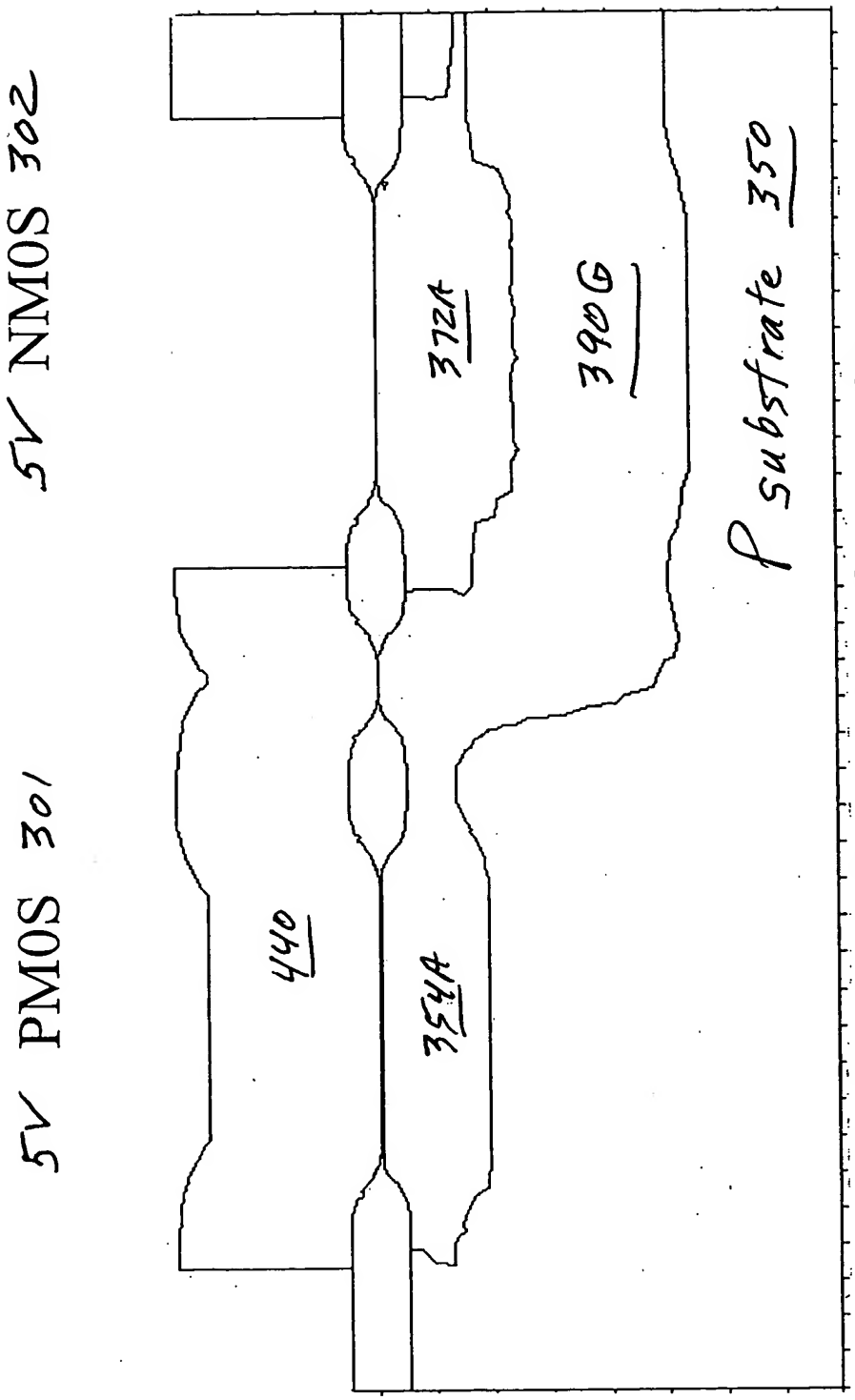
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



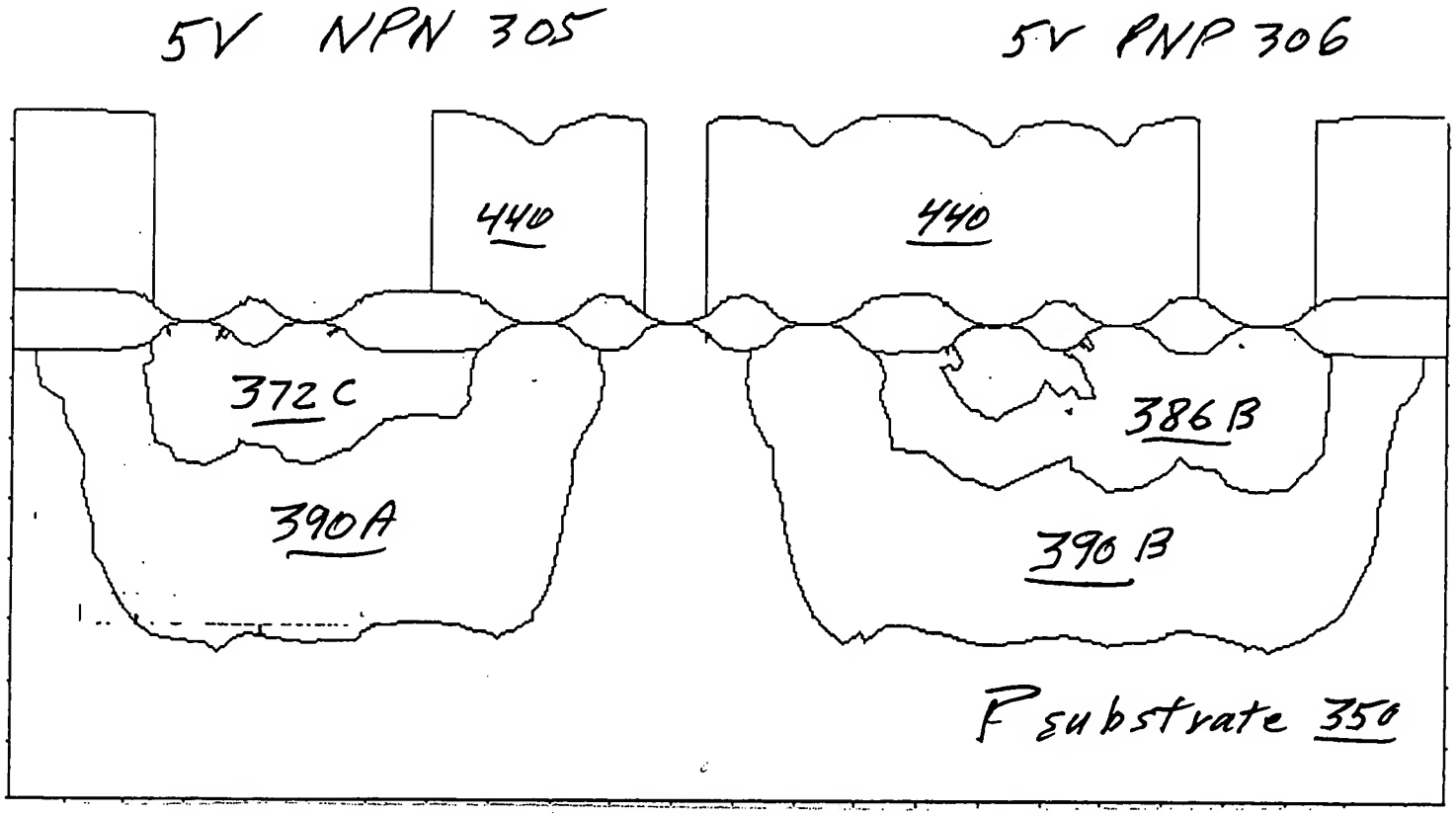
5V P Well Implant – First Stage

Fig. 45E



5V P Well Implant - Second Stage
Fig 2 46A

High F_T Layout

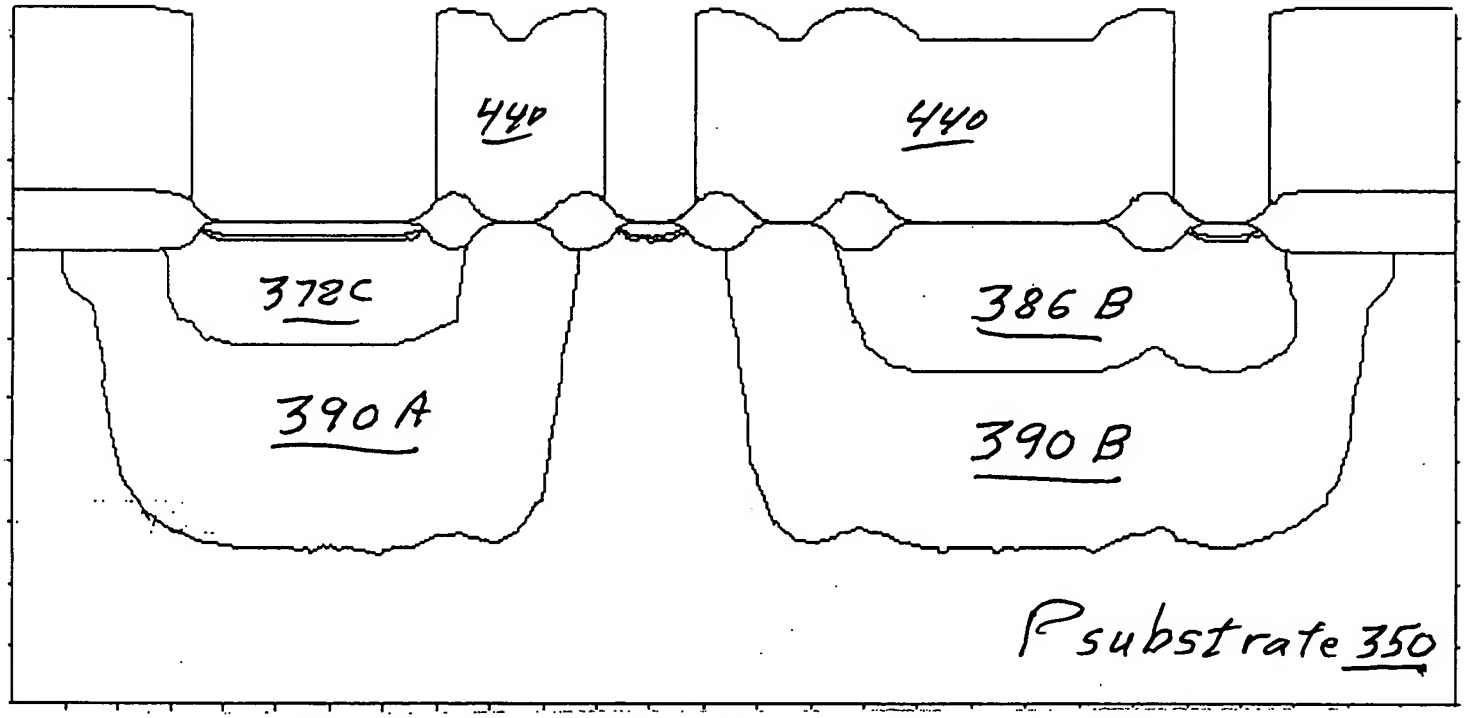


5V P Well Implant - Second Stage

Fig. 46B

Conventional Layout

5V NPN 305 5V PNP 306

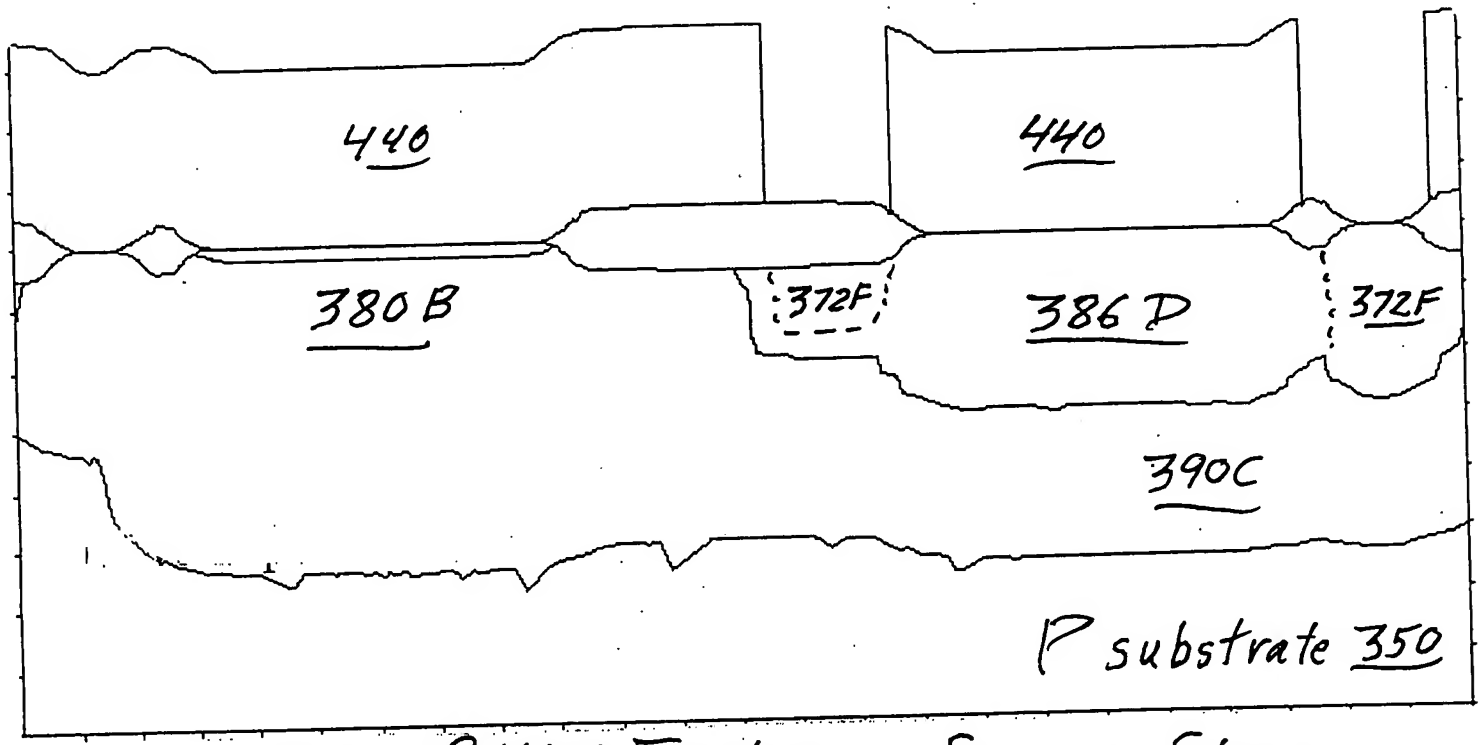


5V P Well Implant - Second Stage

Fig. 46C

Symmetrical 12V CMOS

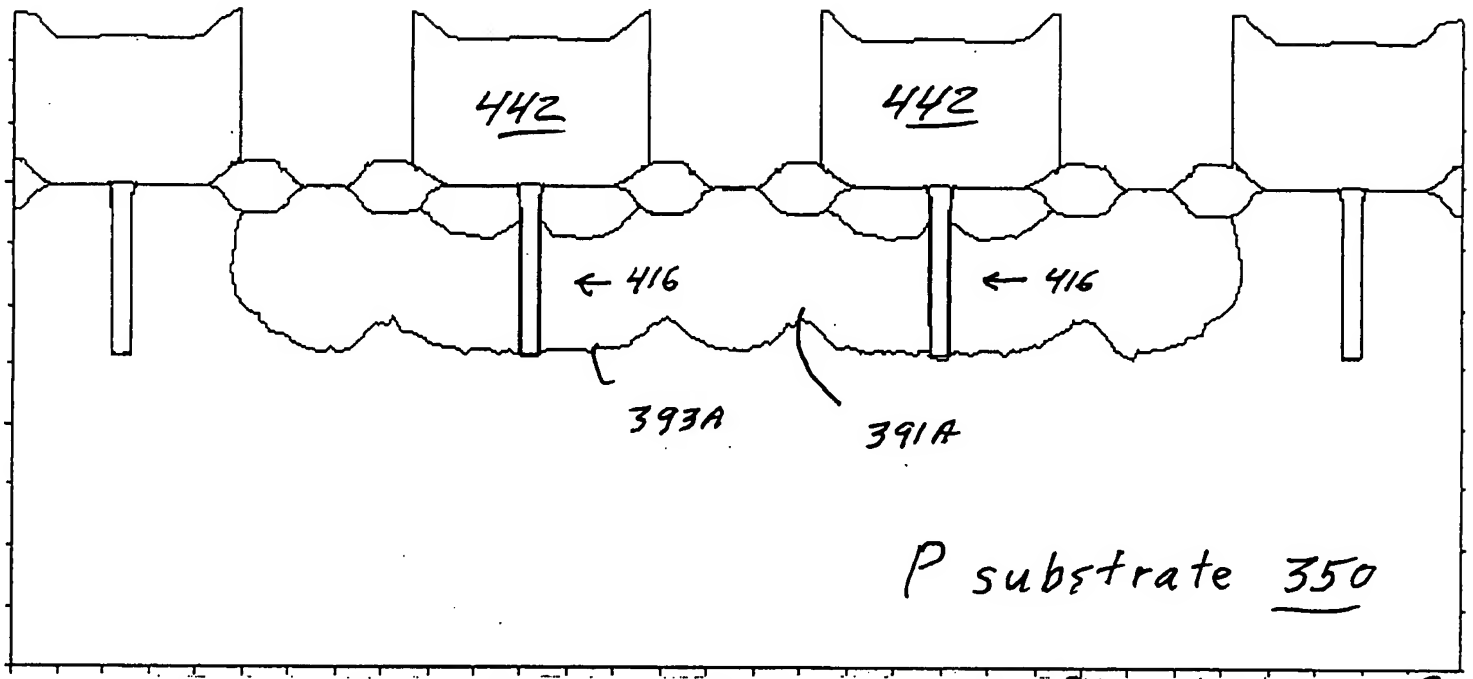
12V PMOS 309 12V NMOS 310



5V P Well Implant – Second Stage

Fig. 46E

30V Lateral Trench DMOS 308



Etch - Block Mask and Etching of Planar Active Regions

Fig. 47D

5V PMOS 301

5V NMOS 302

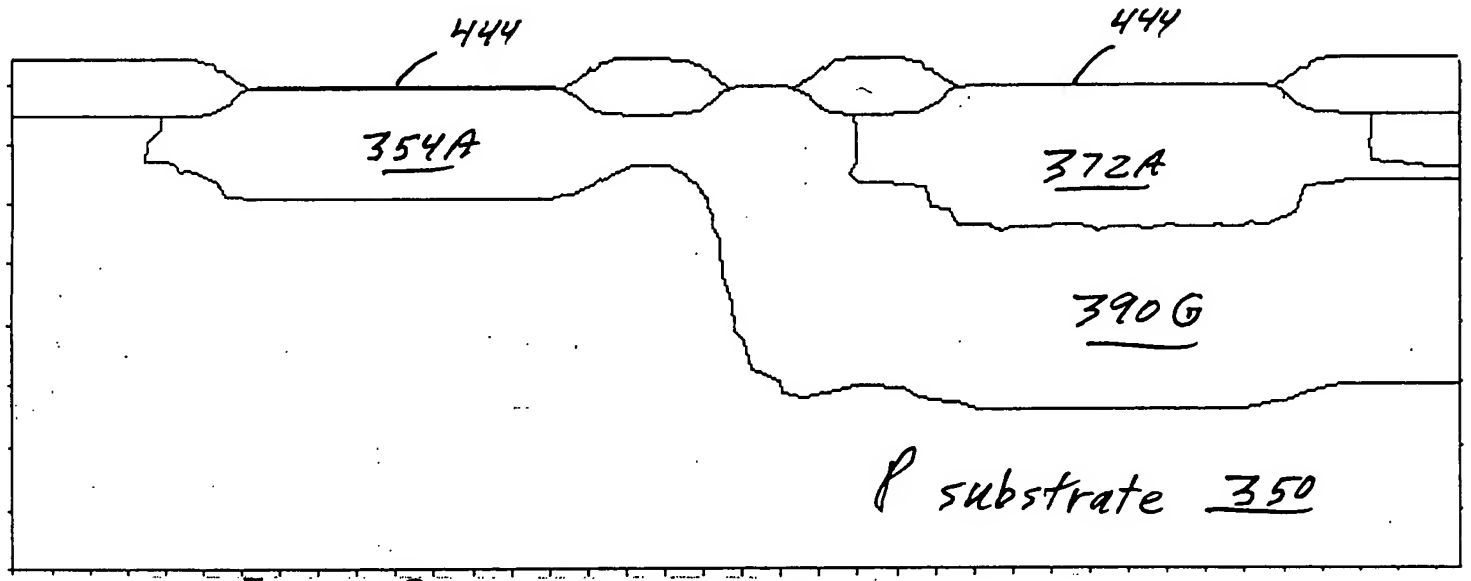
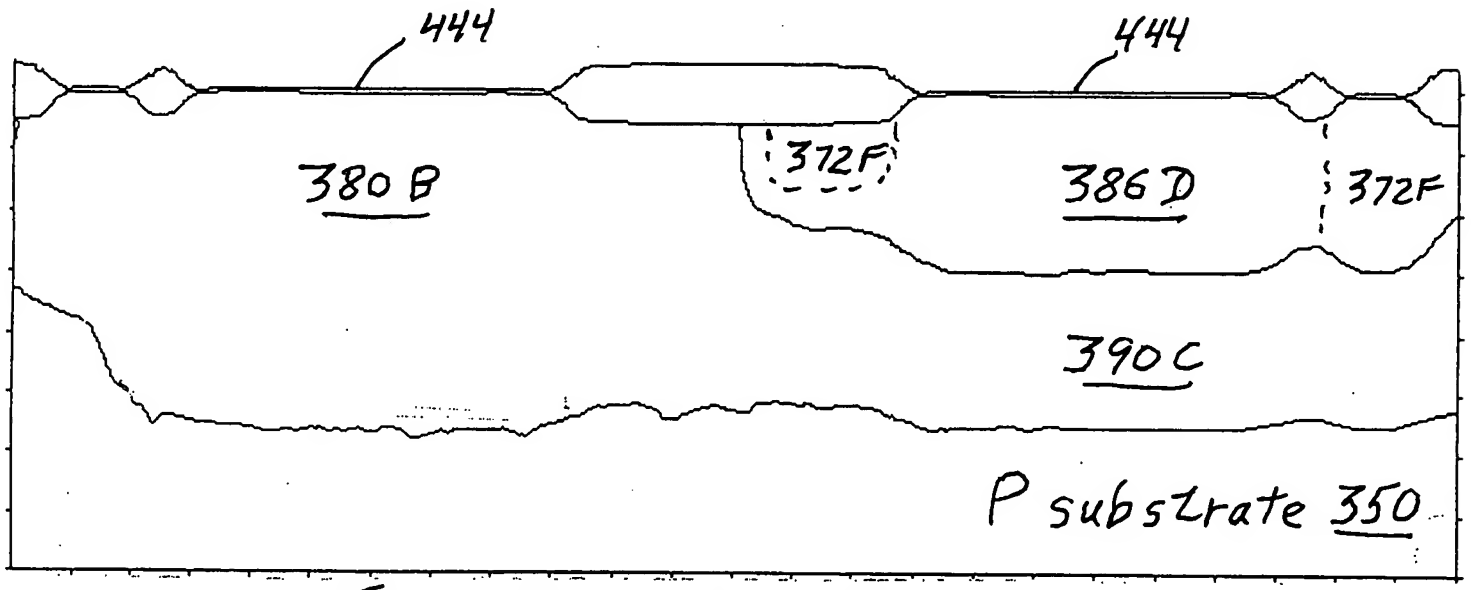


Fig. 4BA

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

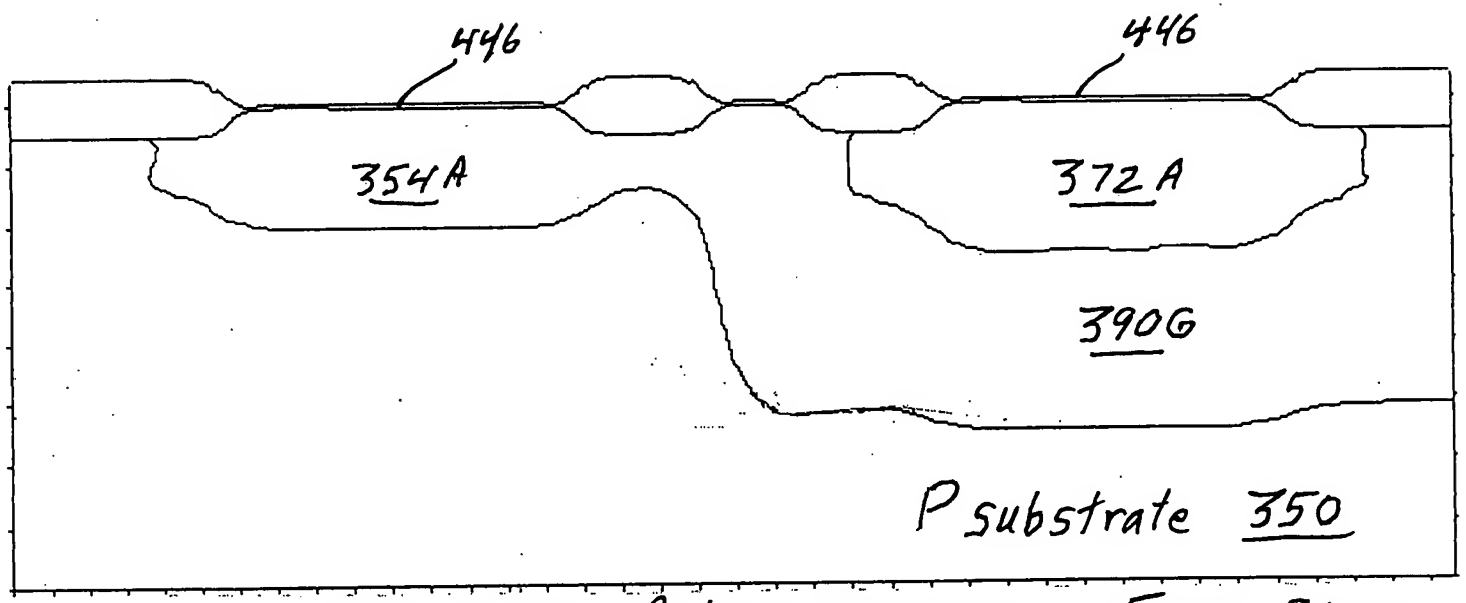


First Planar Gate Oxide

Fig 48E

612/251

5V PMOS 301 5V NMOS 302

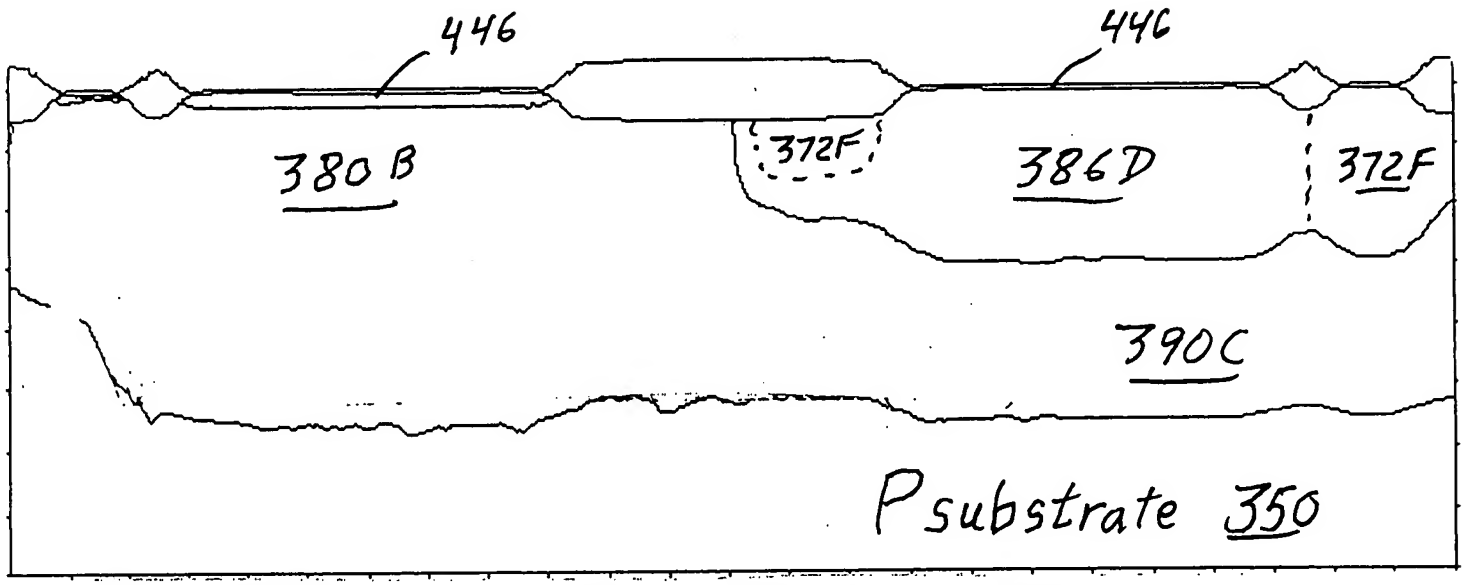


Threshold Adjust Implant - First Stage

Fig. 49A

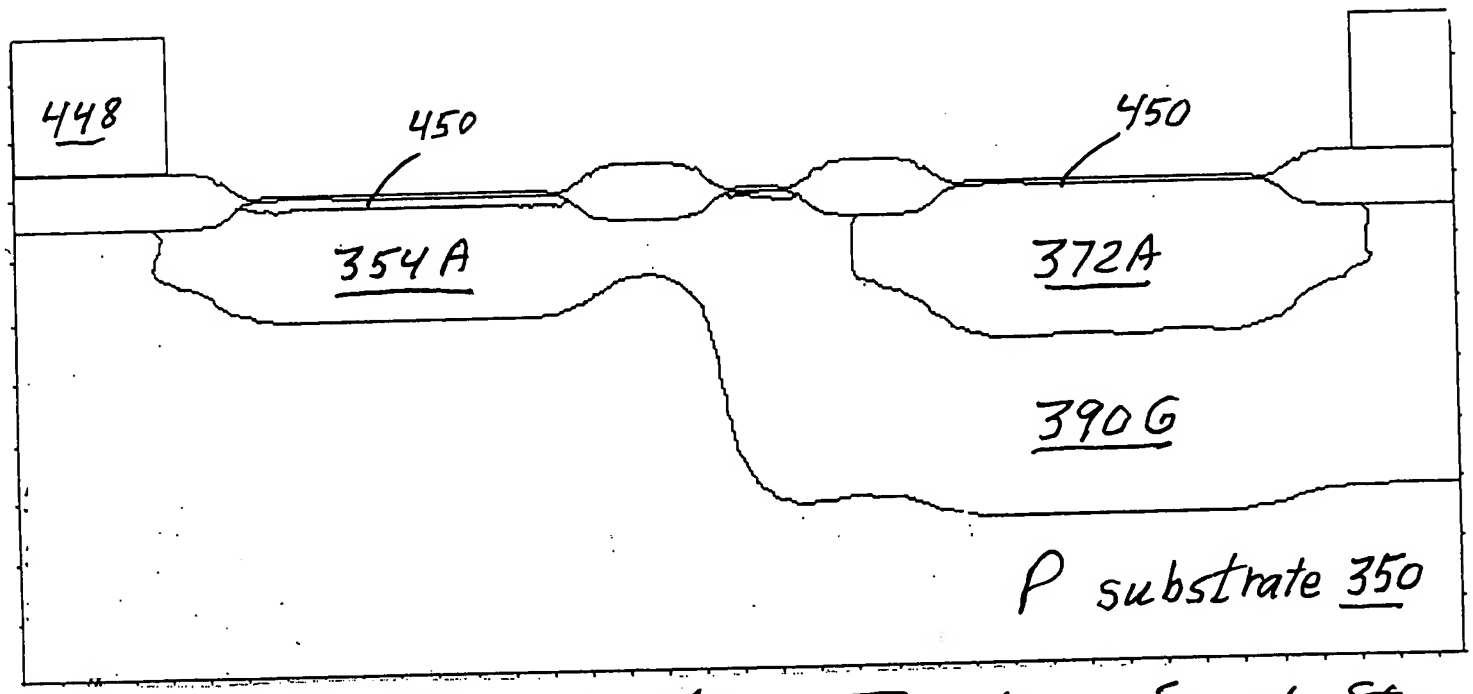
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Threshold Adjust Implant – First Stage

Fig. 49E

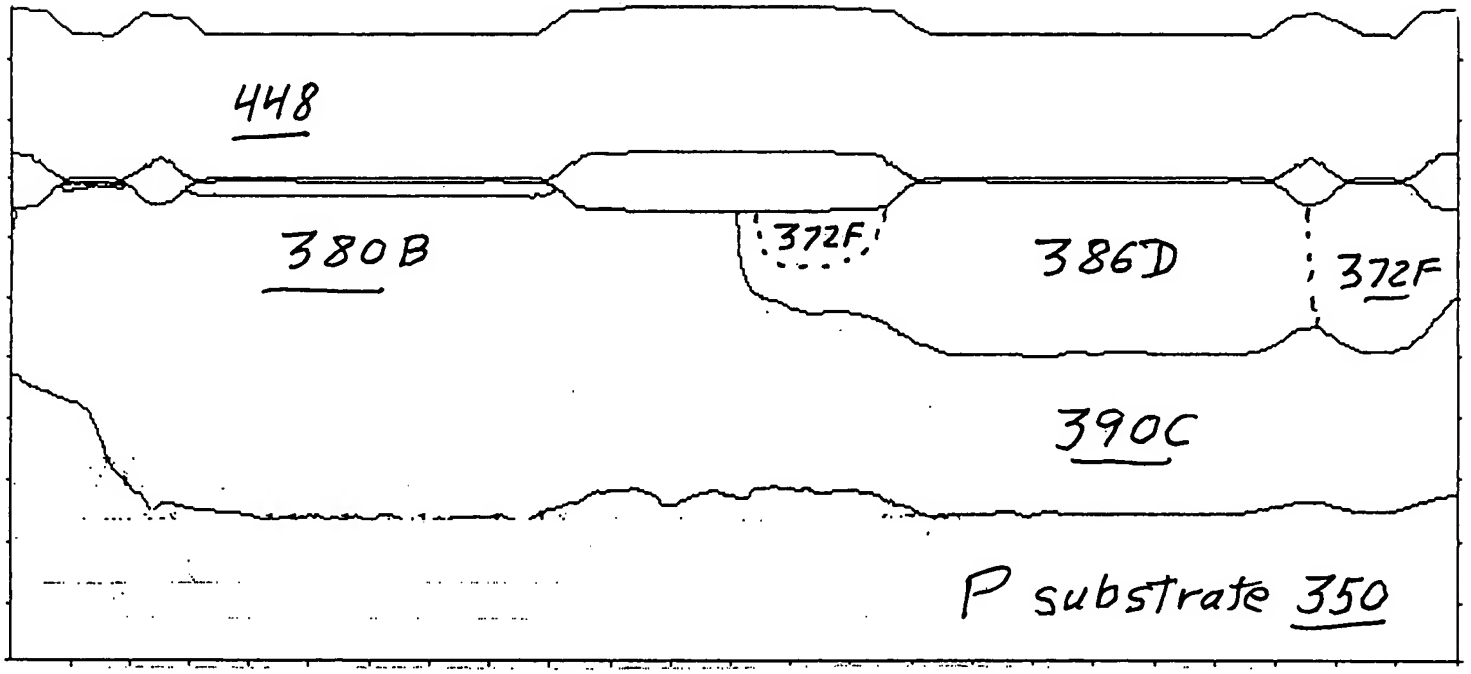


Threshold Adjust Implant - Second Stage
First Planar Gate Oxide Removal

Fig. 50A

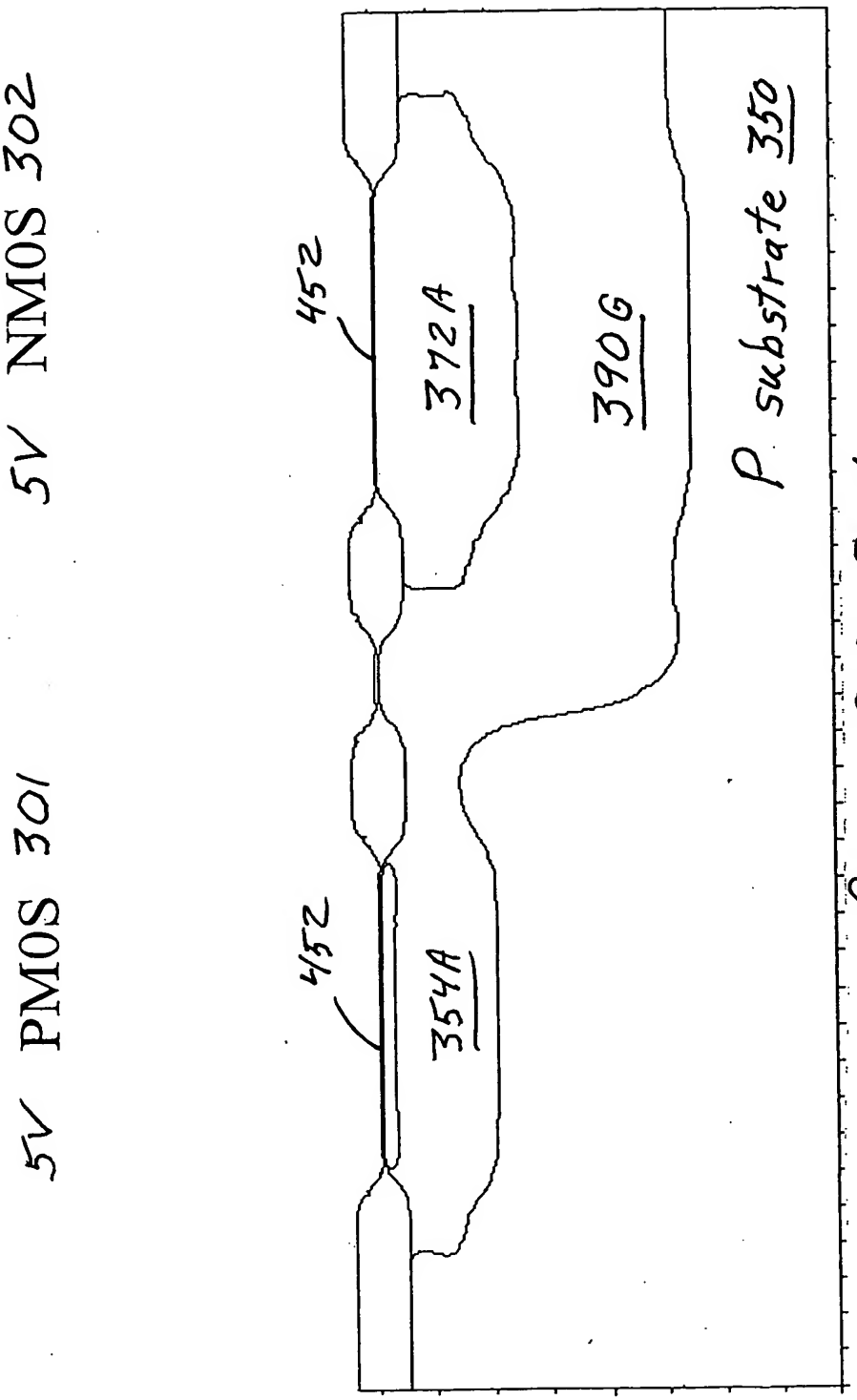
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Threshold Adjust Implant - Second Stage

Fig. 50E



Second Planar Gate Oxide
Fig. 5IA

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

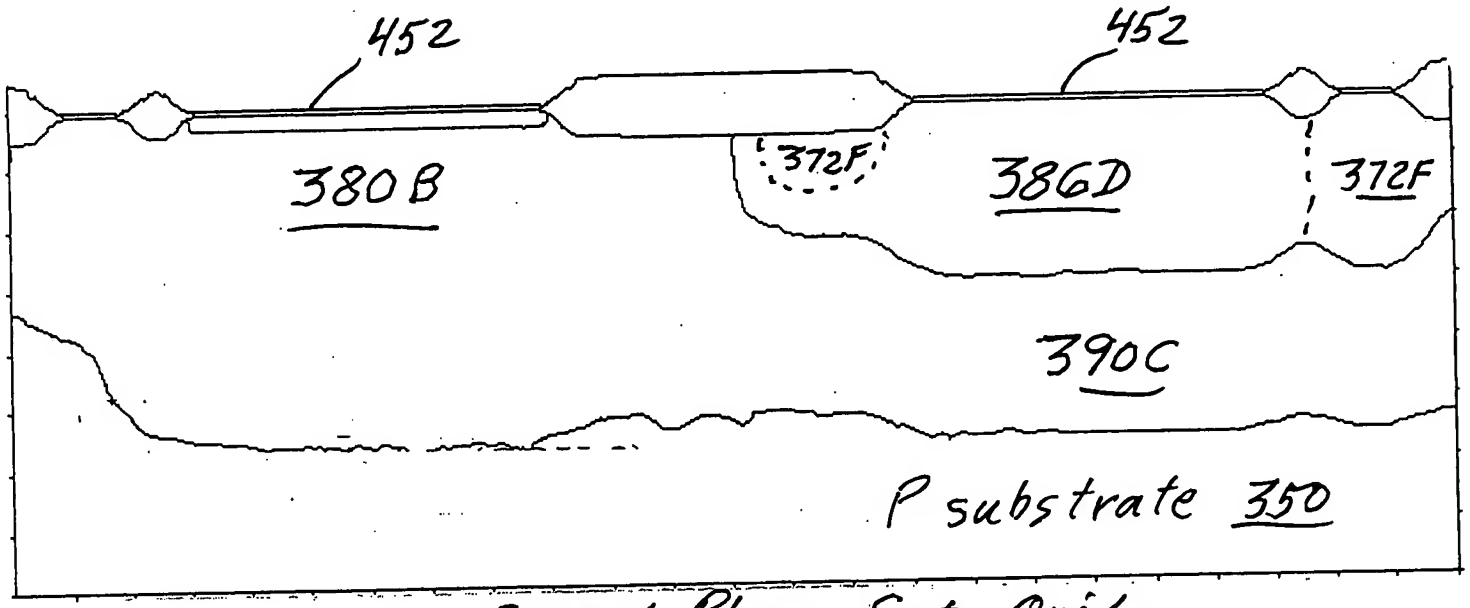
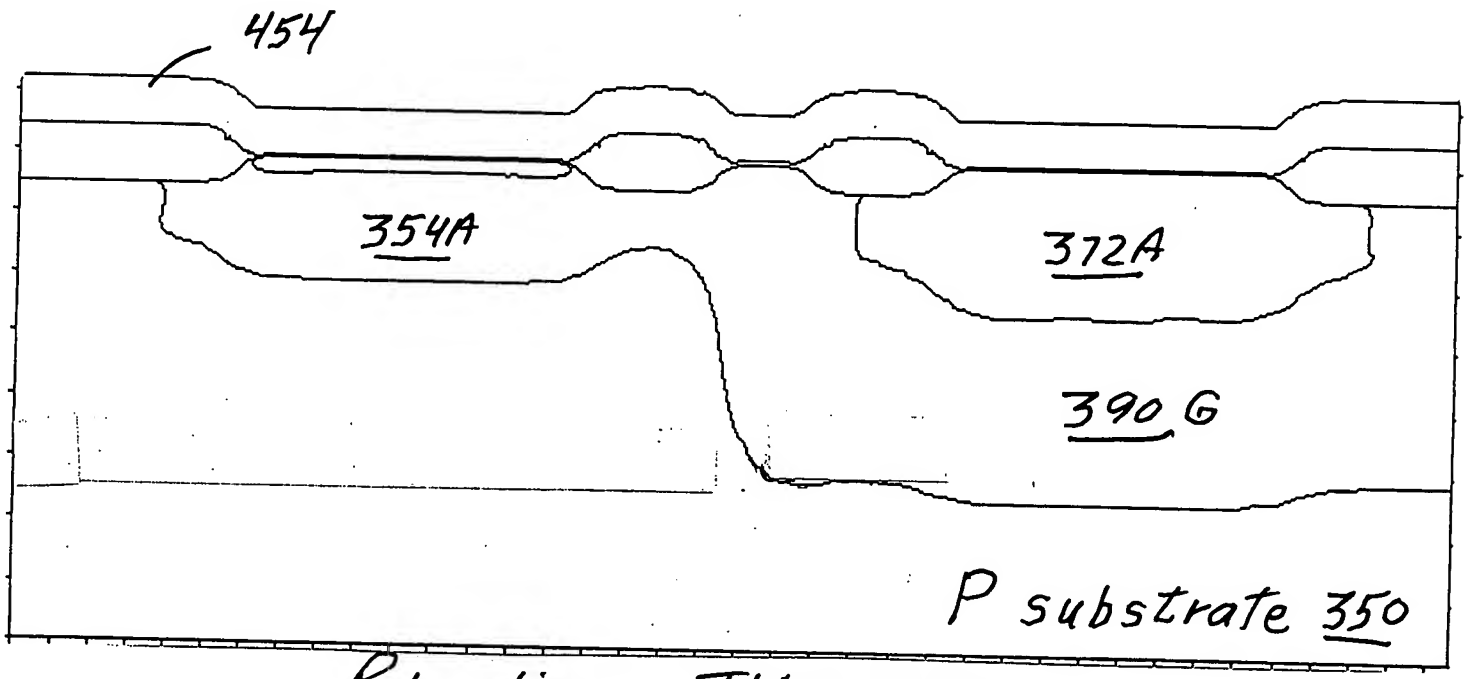


Fig. 5E

612/851

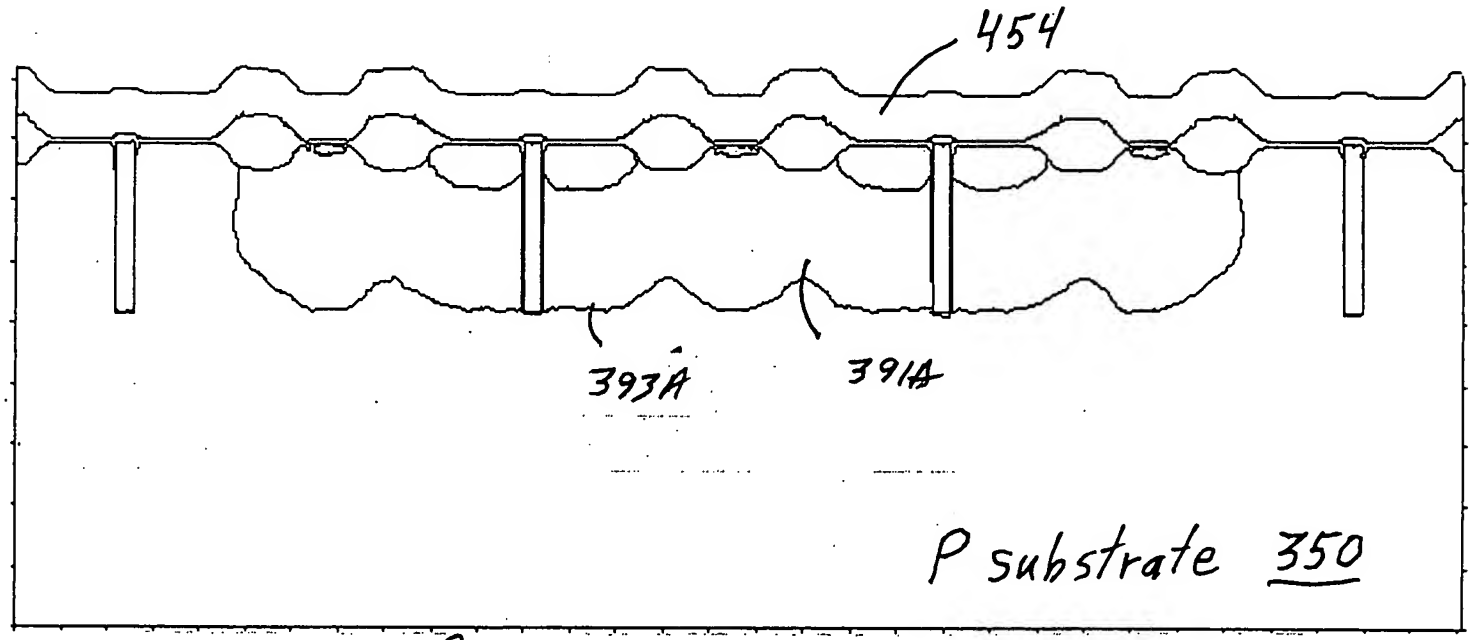
5V PMOS 301 5V NMOS 302



Polysilicon - Third Layer

Fig. 52A

30V Lateral Trench DMOS 308

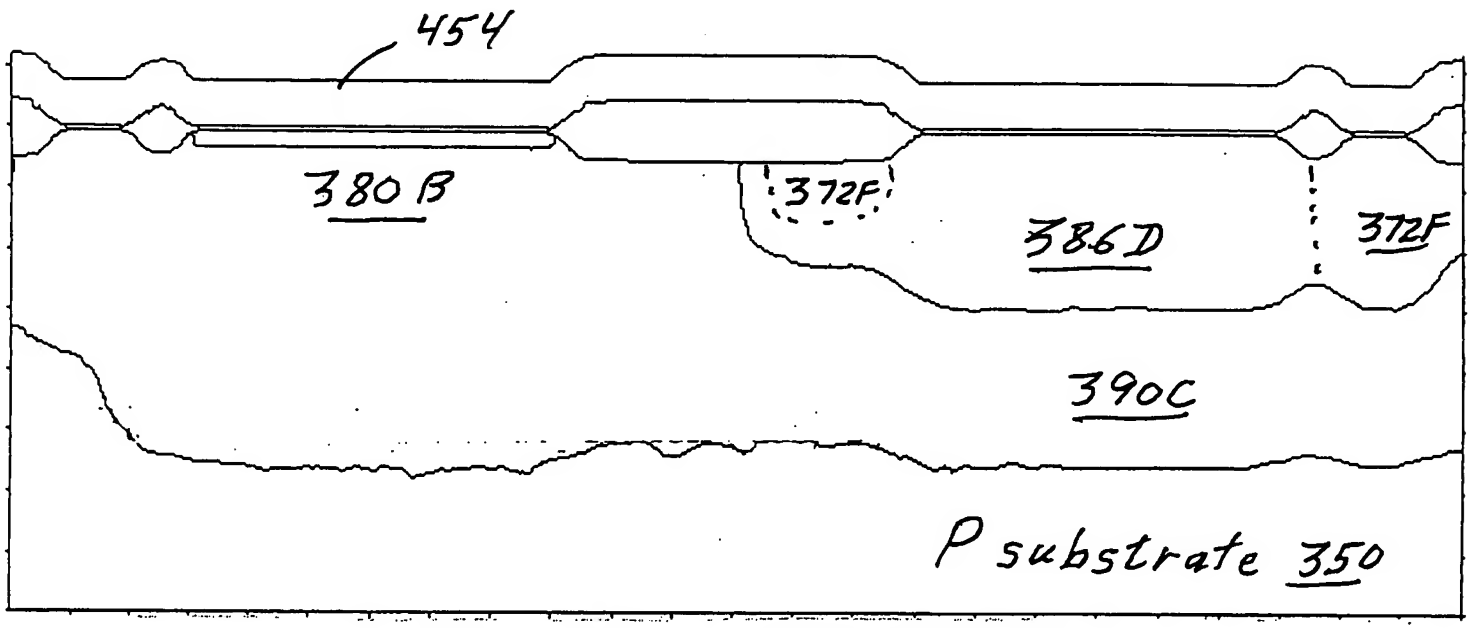


Polysilicon – Third Layer

Fig. 52D

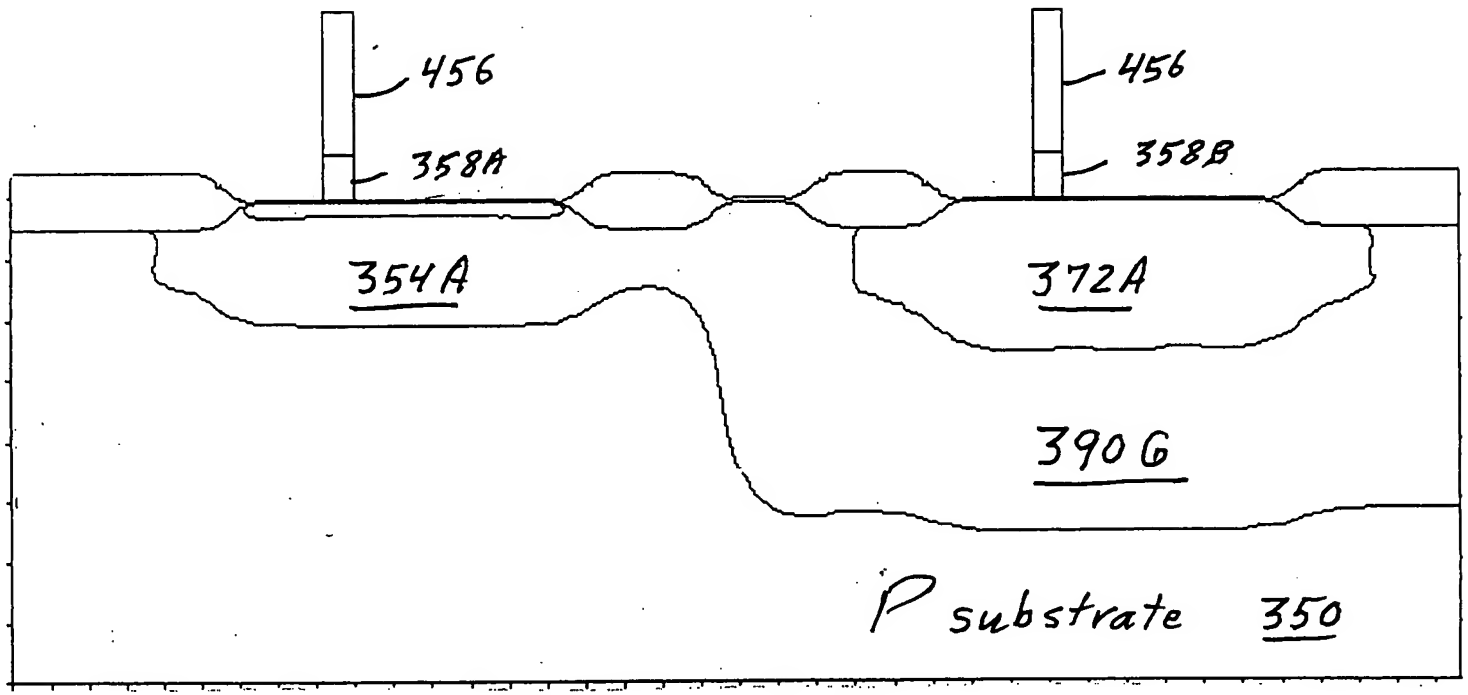
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Polysilicon - Third Layer

Fig. 52E



Planar Gate Formation

Fig. 5-3A

30V Lateral Trench DMOS 308

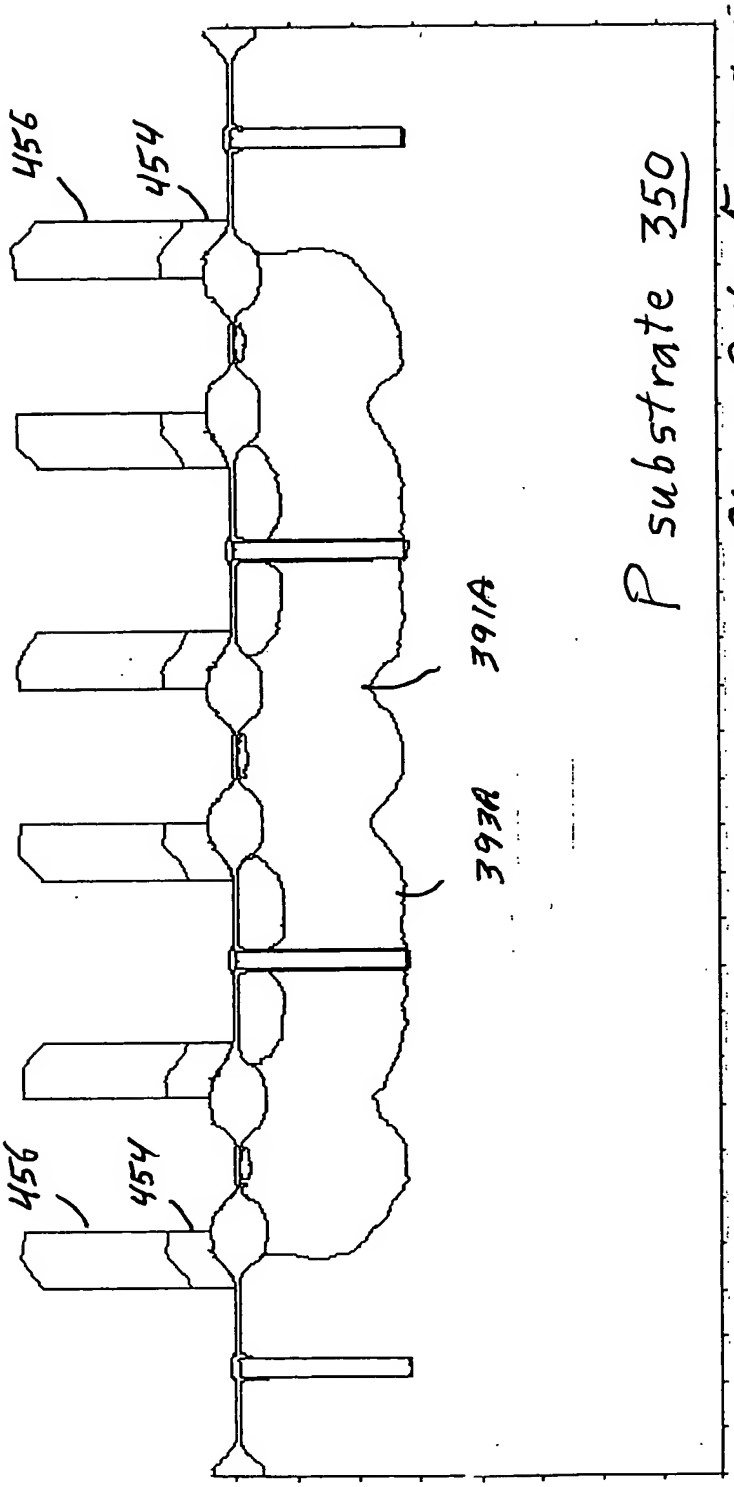
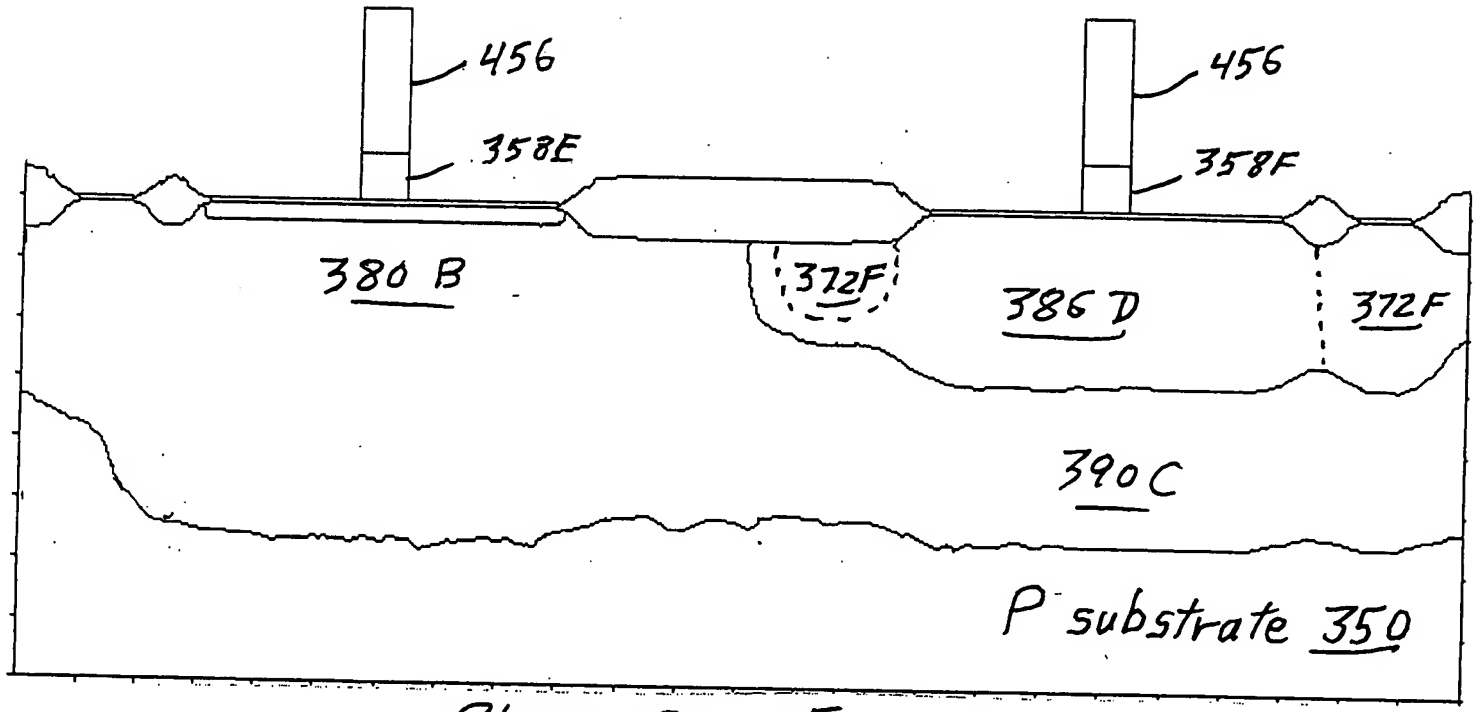


Fig. 3D Planar Gate Formation

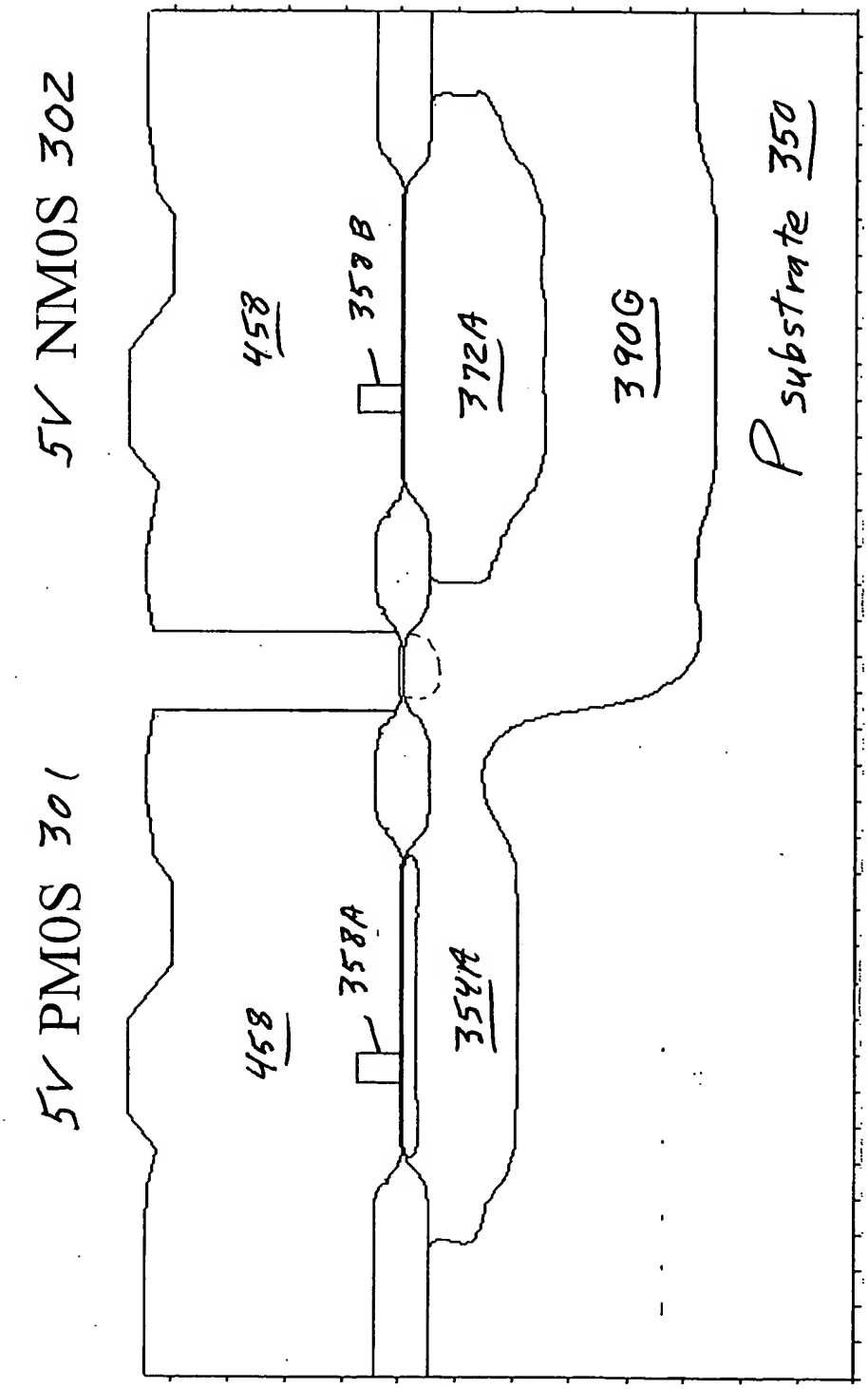
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Planar Gate Formation

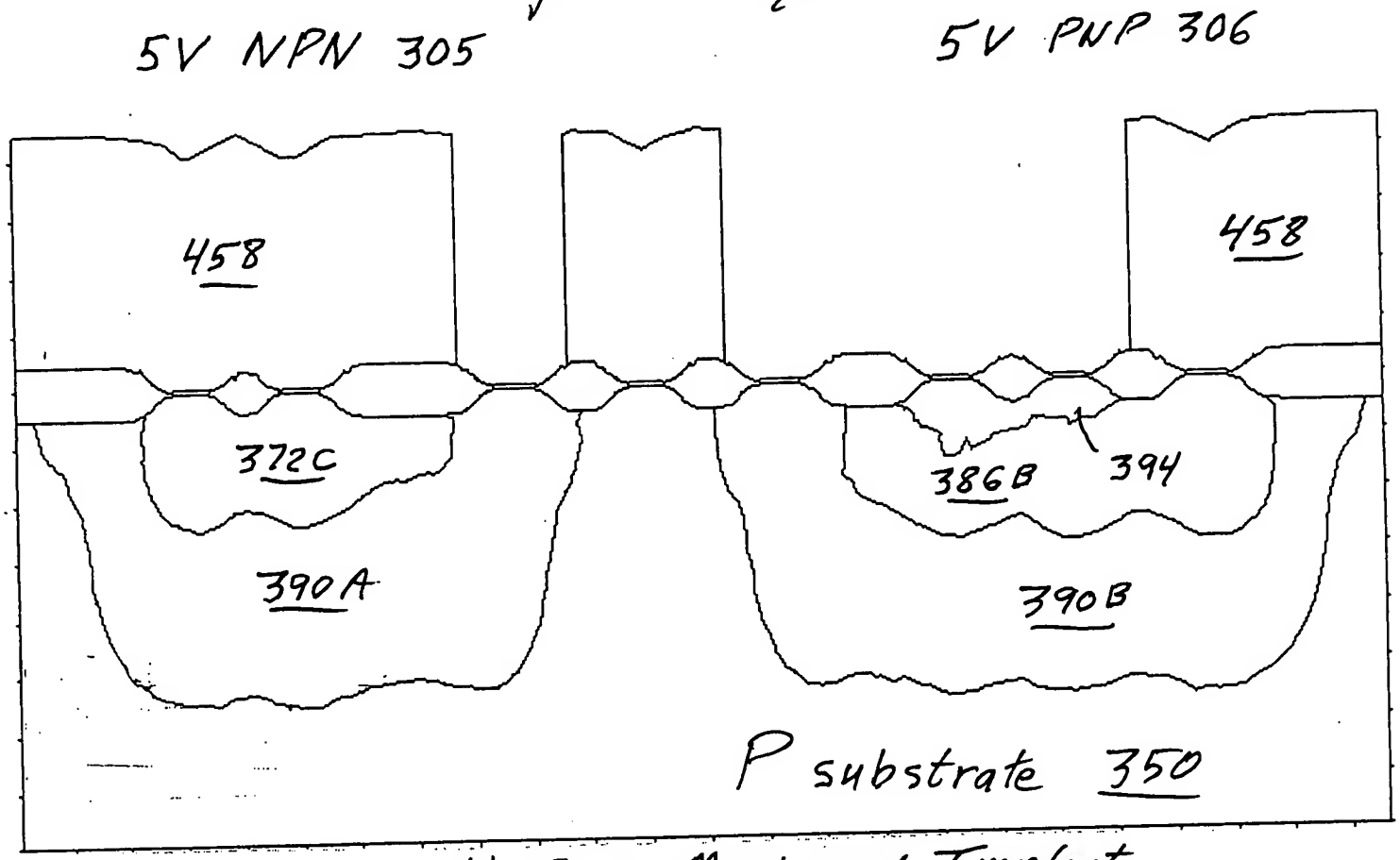
Fig 53E



N-Base Mask and Implant

Fig. 54A

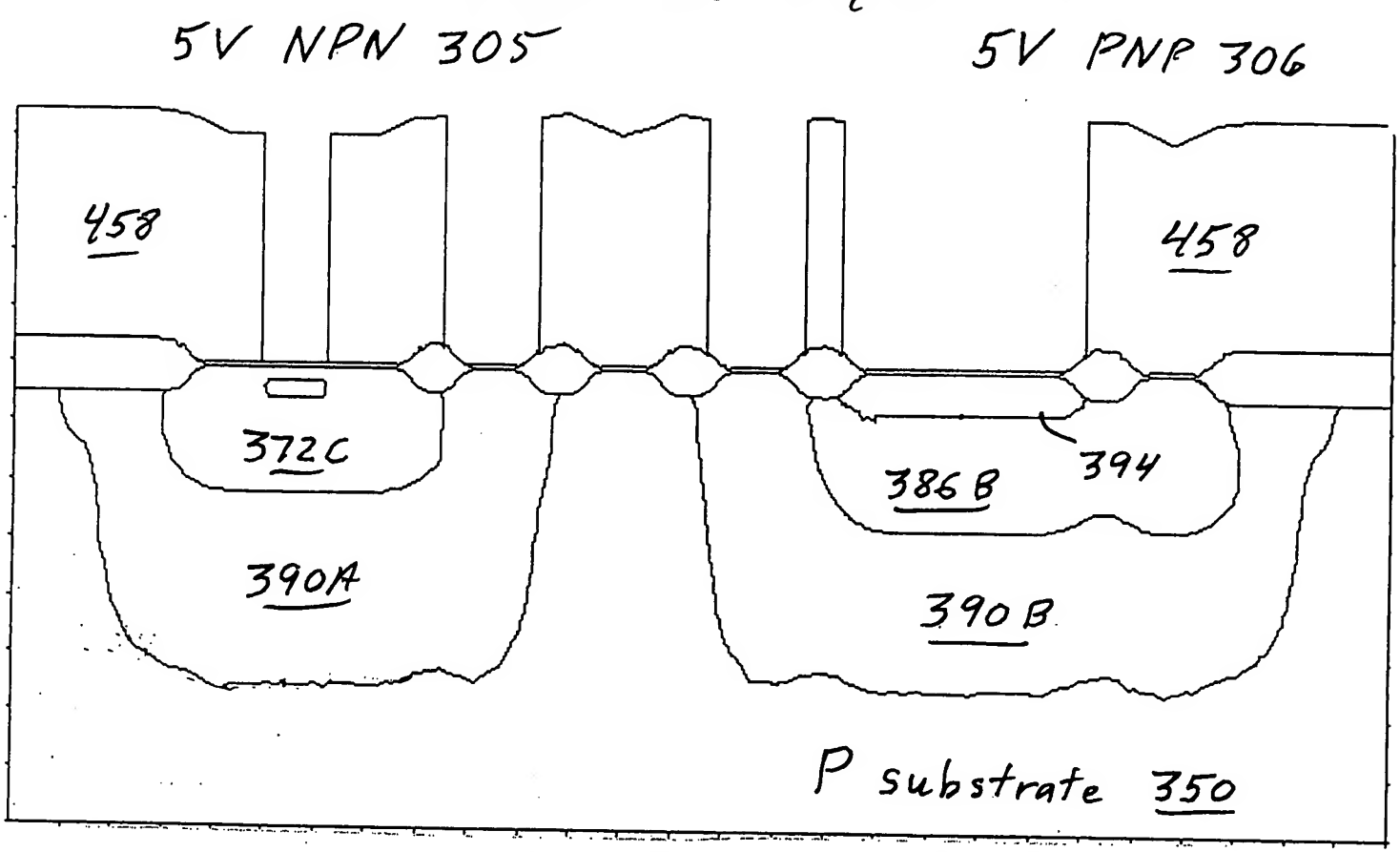
High F_T Layout



N-Base Mask and Implant

Fig. 54B

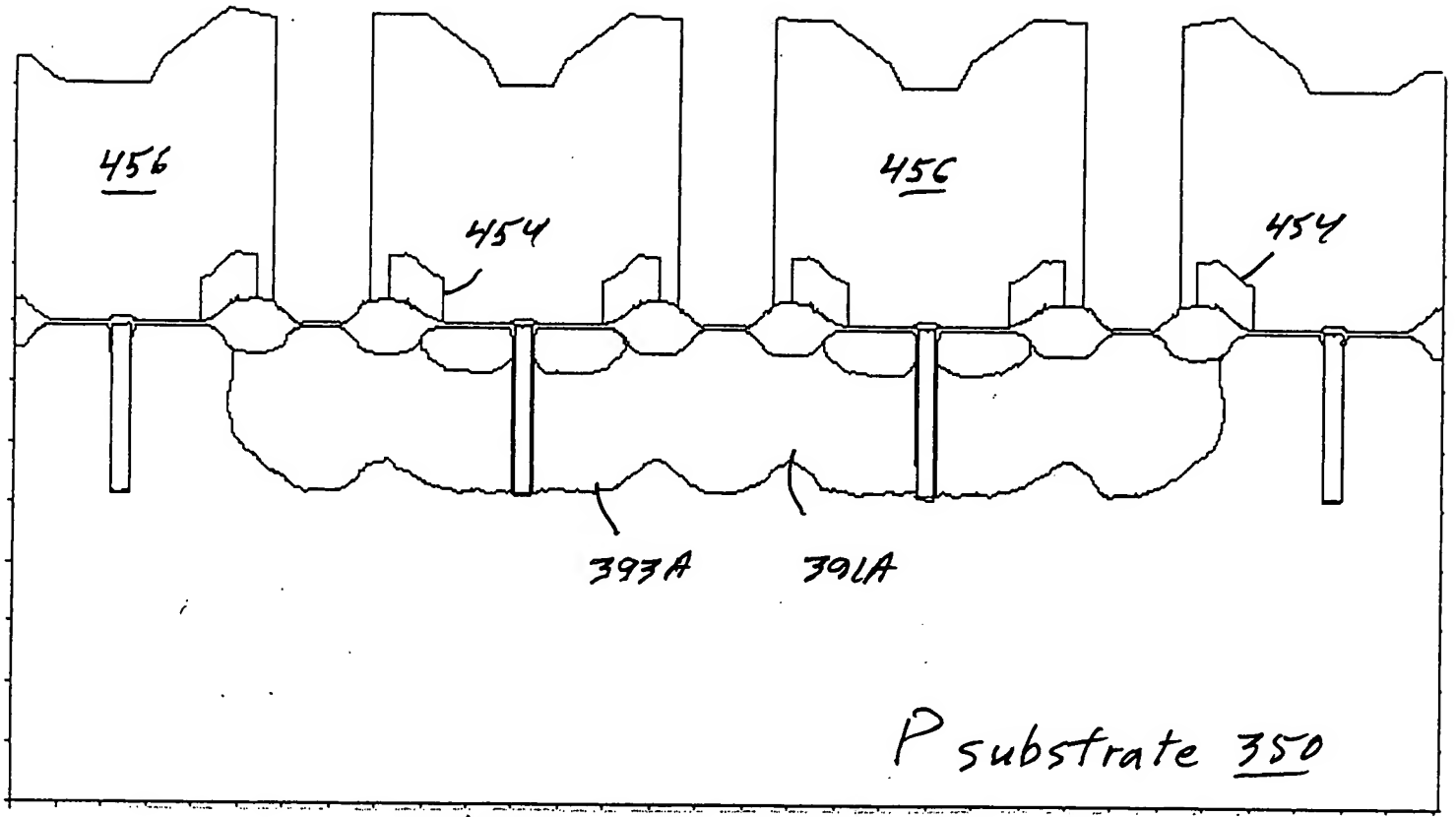
Conventional Layout



N-Base Mask and Implant

Fig. 54C

30V Lateral Trench DMOS 308

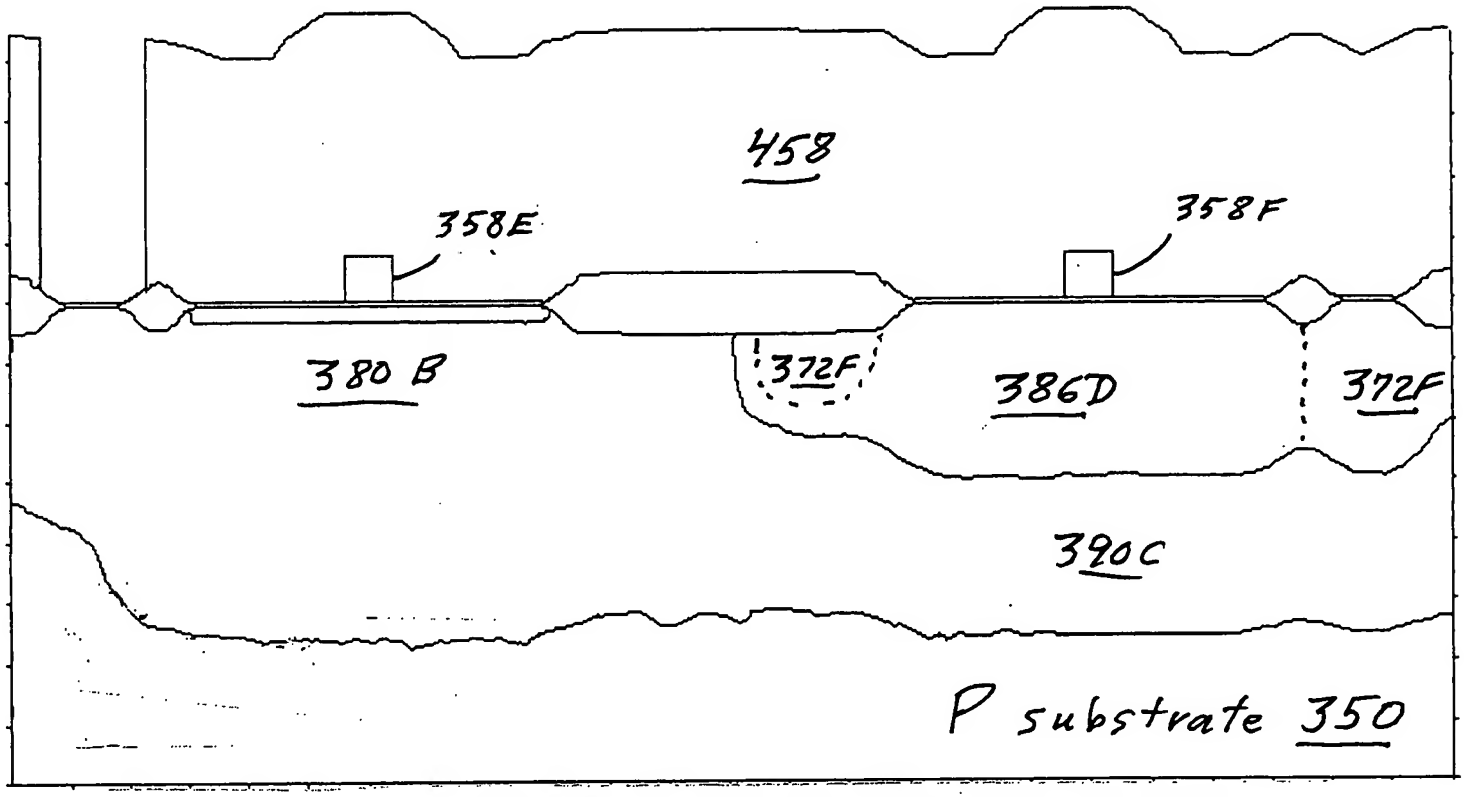


N-Base Mask and Implant

Fig. 54D

Symmetrical 12V CMOS

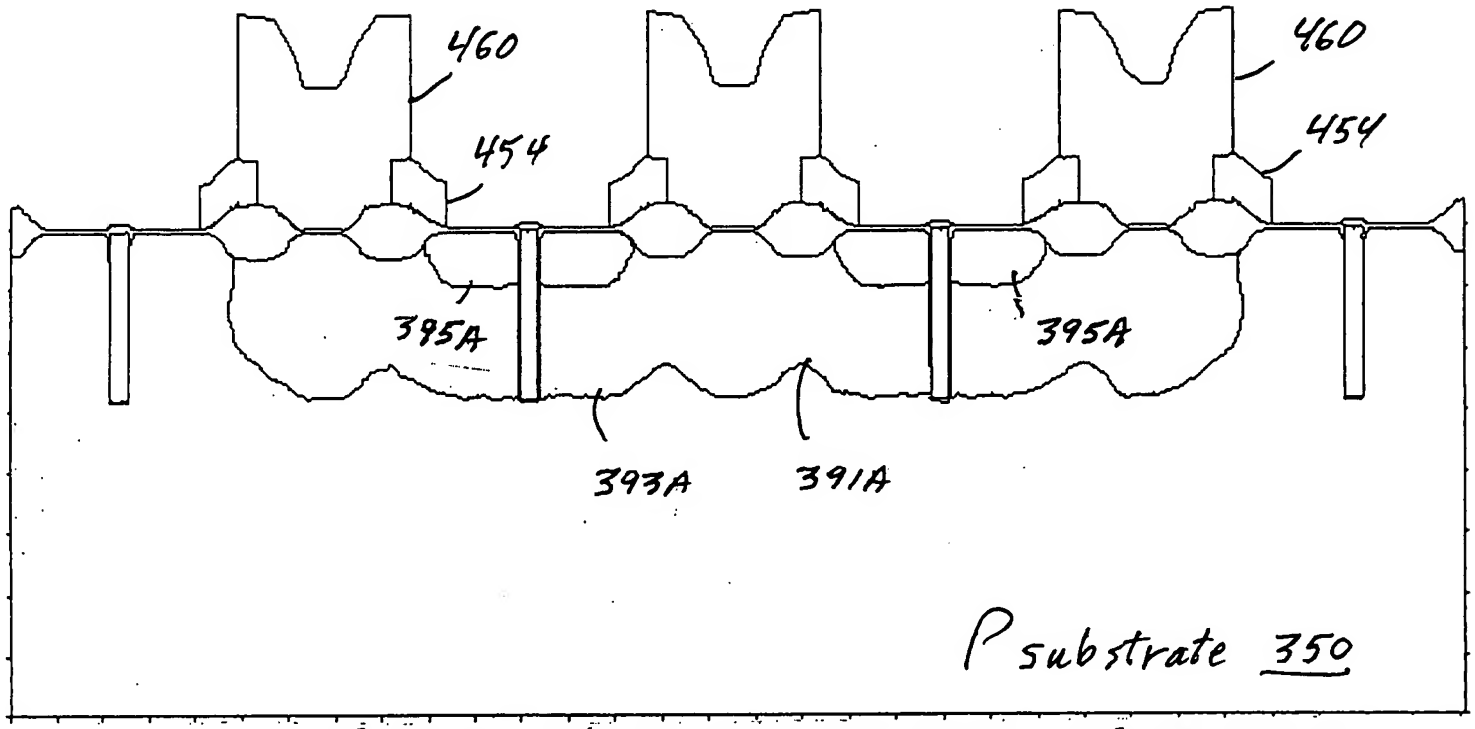
12V PMOS 309 12V NMOS 310



N- Base Mask and Implant

Fig. 54E

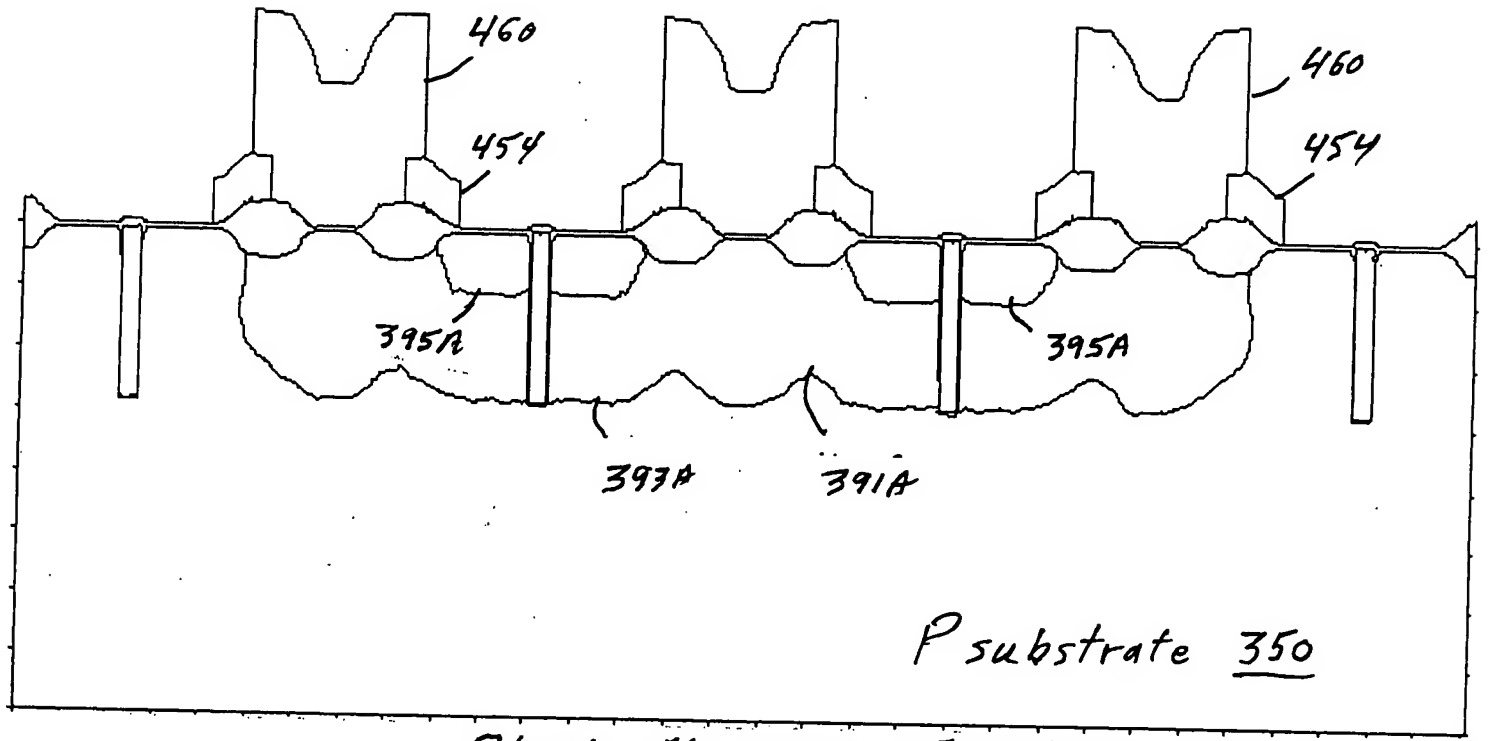
30V Lateral Trench DMOS 308



P Body Mask and Implant - First Stage

Fig. 35D

30V Lateral Trench DMOS 308



Pbody Mask and Implant - Second Stage
Fig. 56D

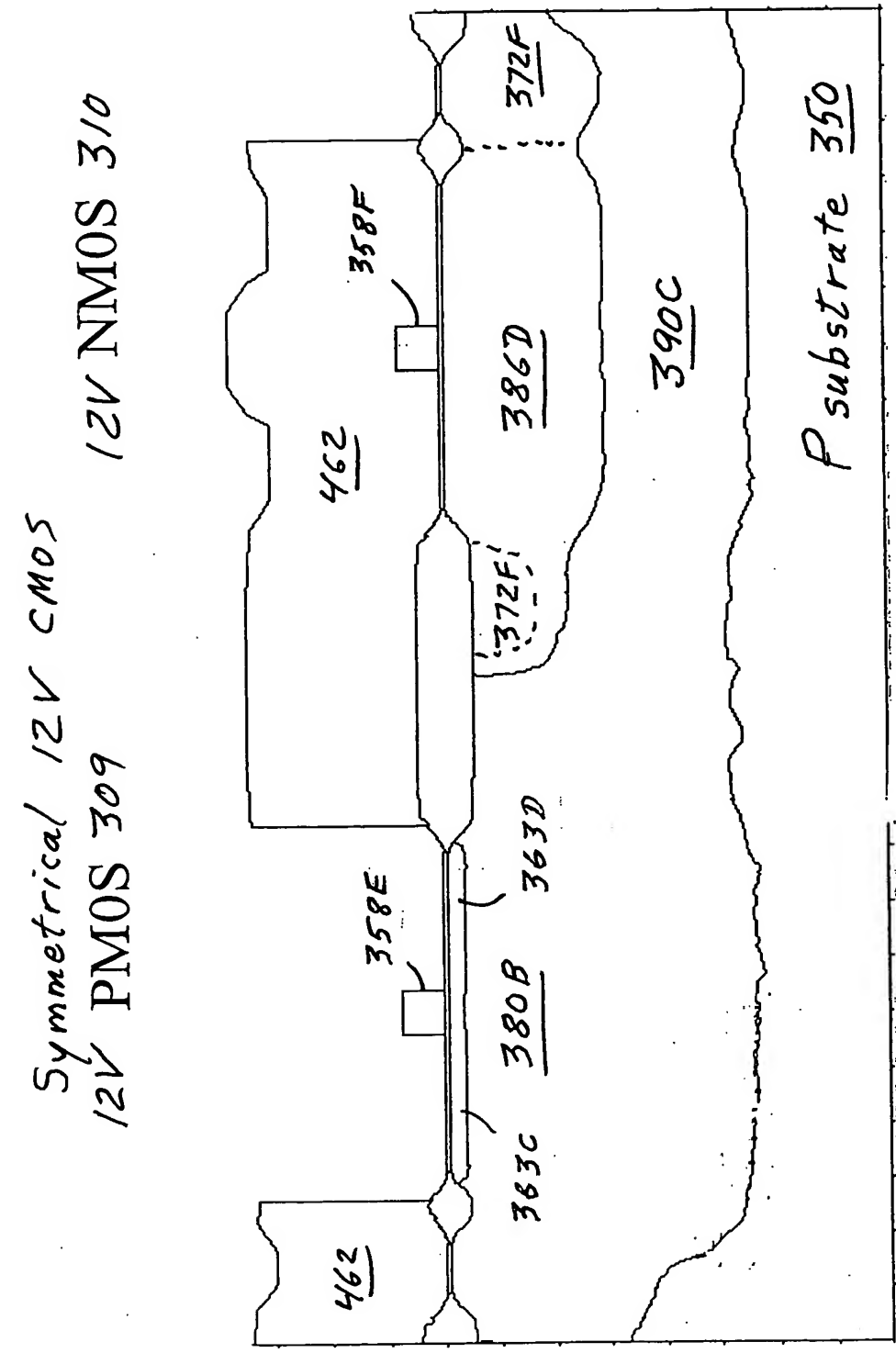
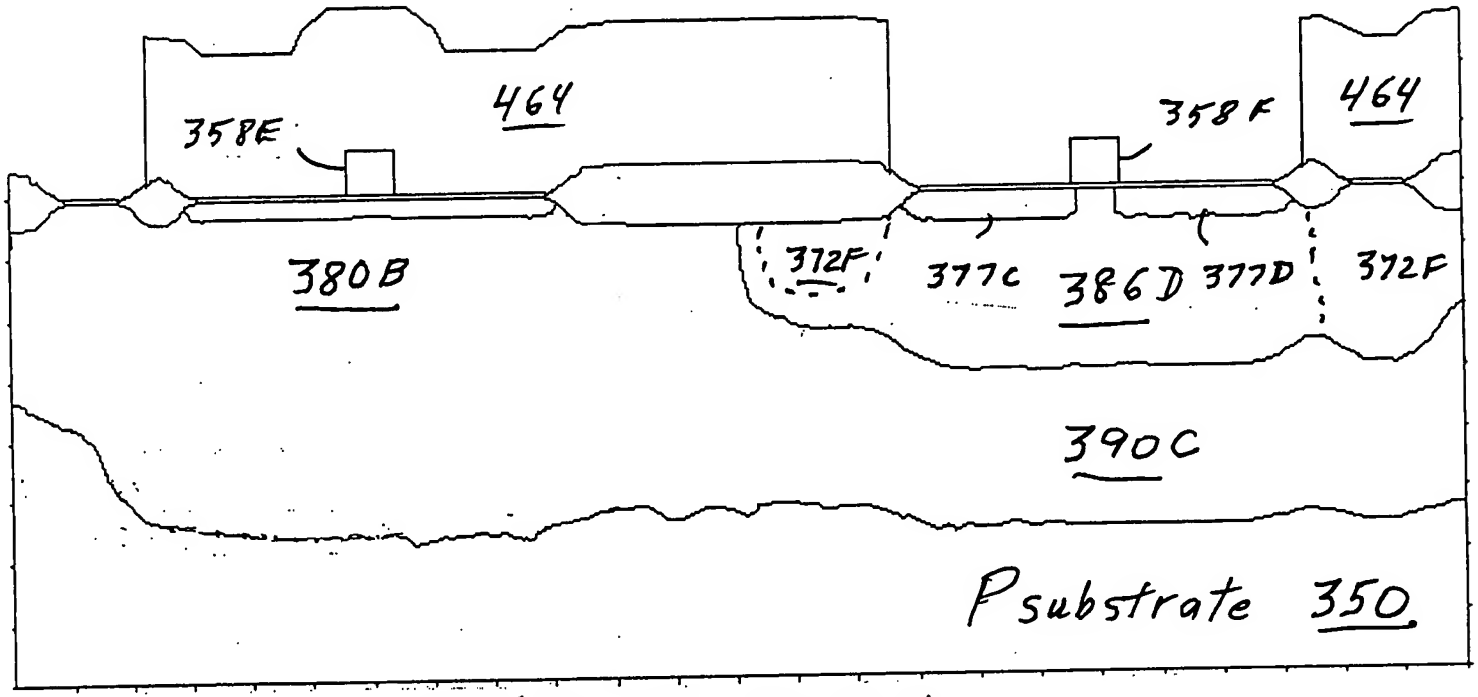

Symmetrical 12V CMOS
12V PMOS 309
12V NMOS 310
462
358F
372F
386D
390C
372F
P substrate 350
358E
363D
380B
363C
462
12V PLDD Implant

Fig. 57E

Symmetrical 12V CMOS

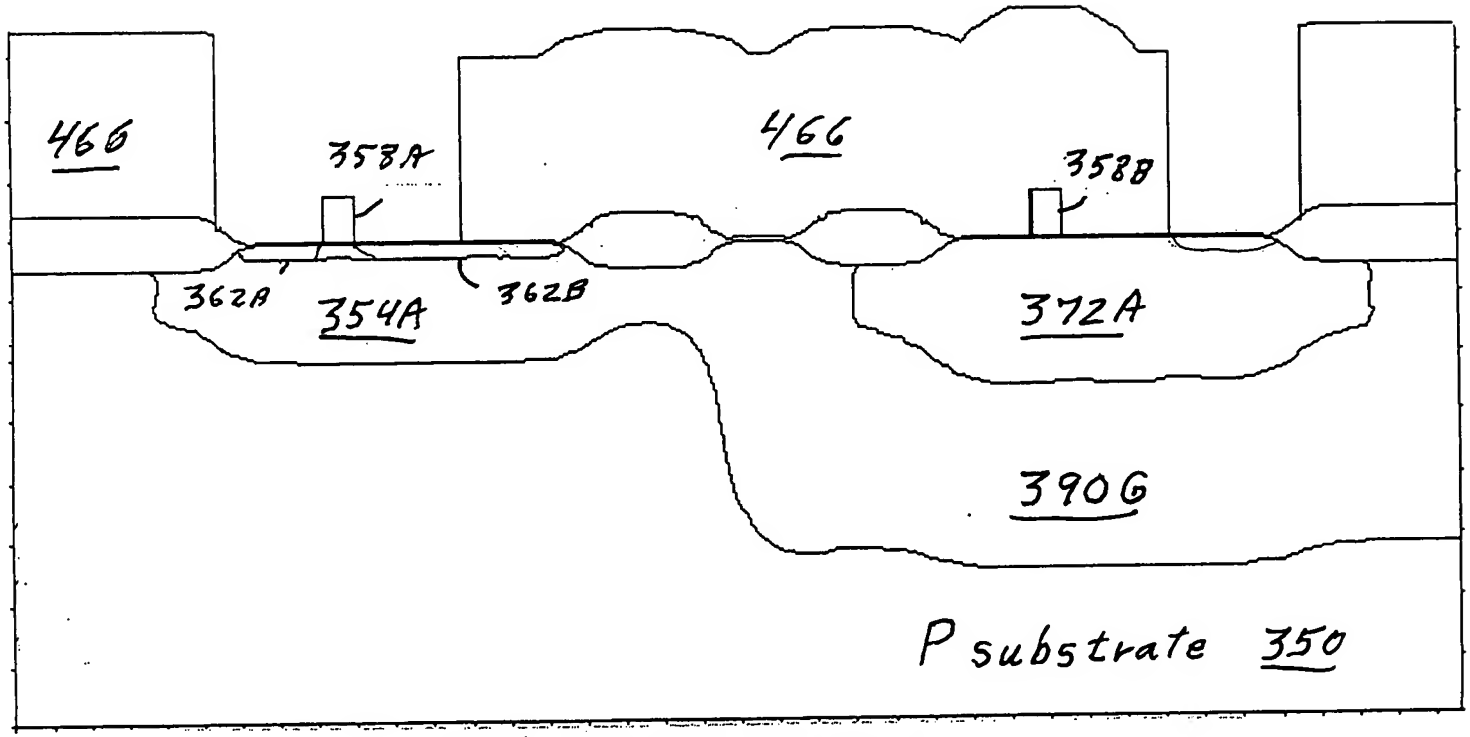
12V PMOS 309 12V NMOS 310



12V N-LDD Implant

Fig. 58E

5V PMOS 301 5V NMOS 302

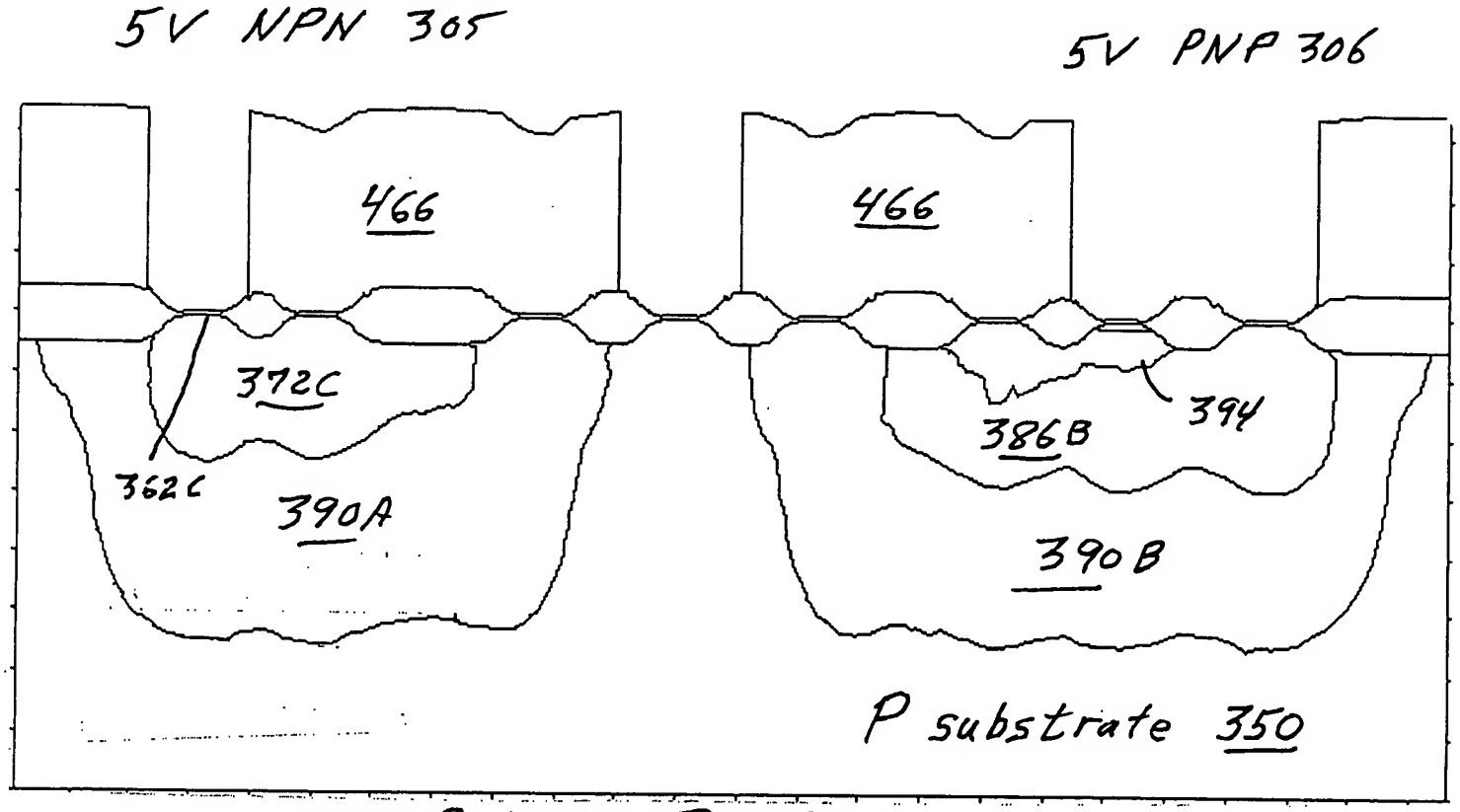


5V P-LDD Implant

Fig. 59A

612/179

High F_T Layout



5V P-LDD Implant

Fig. 59B

Conventional Layout

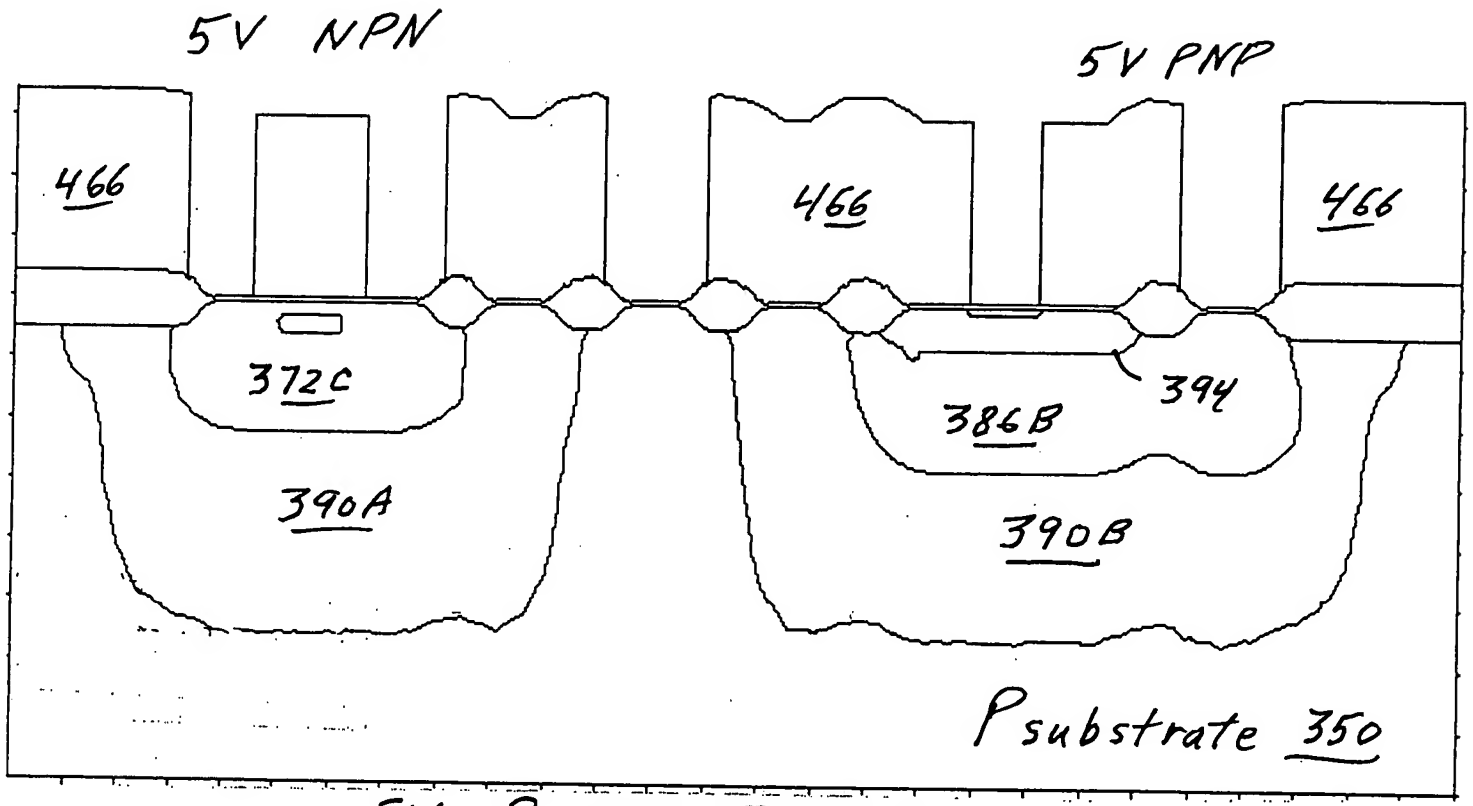
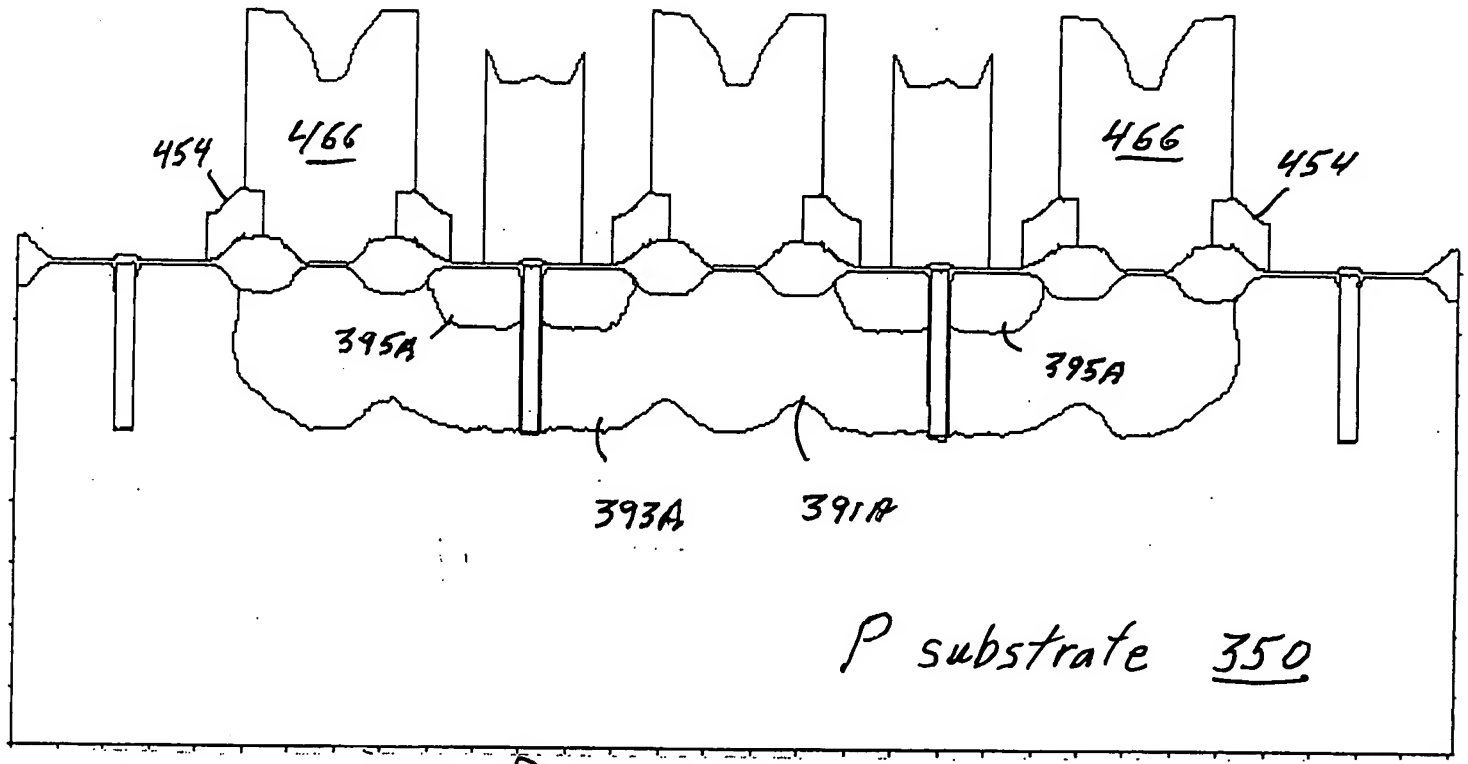


Fig. 59C

30V Lateral Trench DMOS 308



5V P-LDD Implant

Fig. 59D

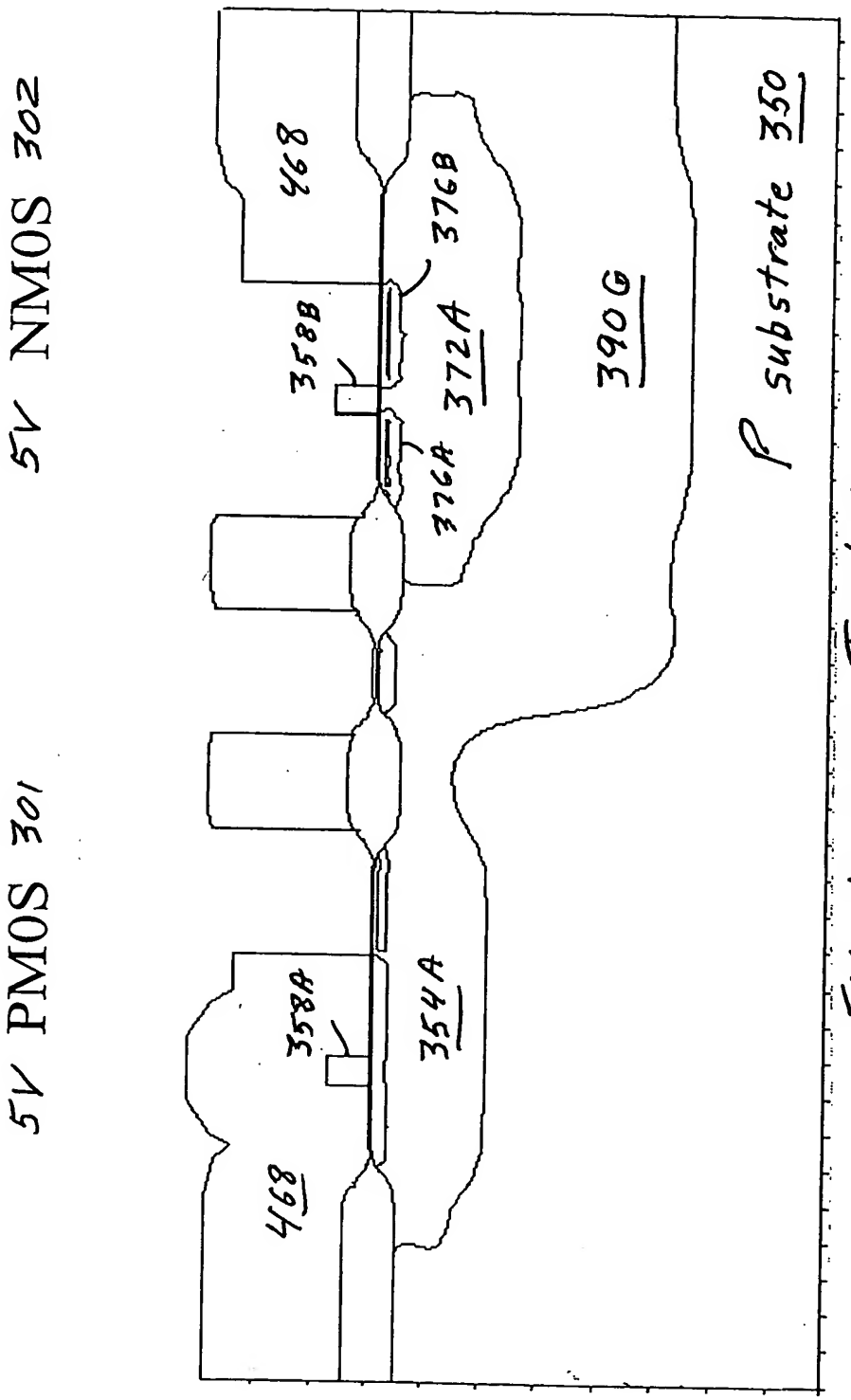
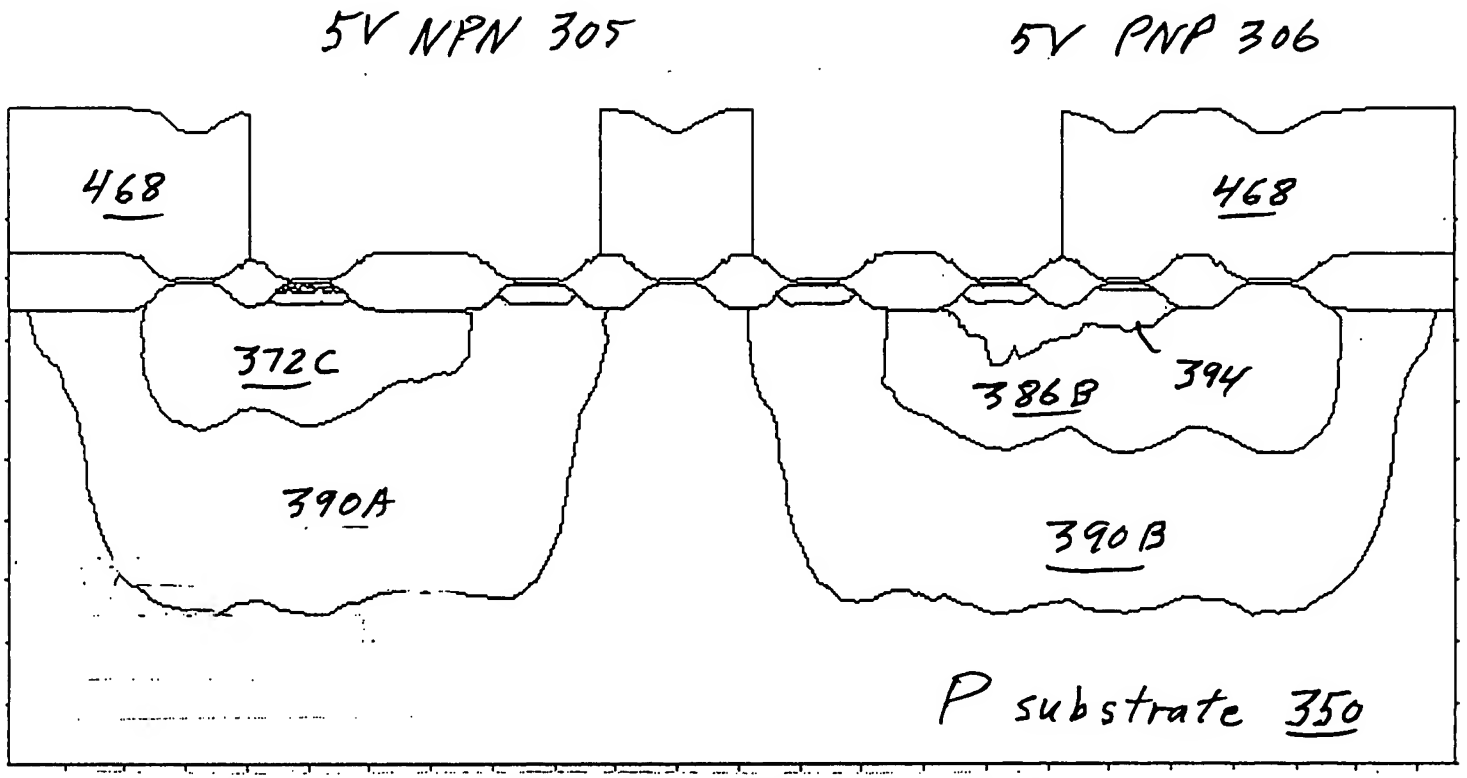

5V PMOS 301
5V NMOS 302
468
376B
358B
372A
376A
390G
P substrate 350
358A
354A
468
5V N-LDD Implant

Fig. 6A

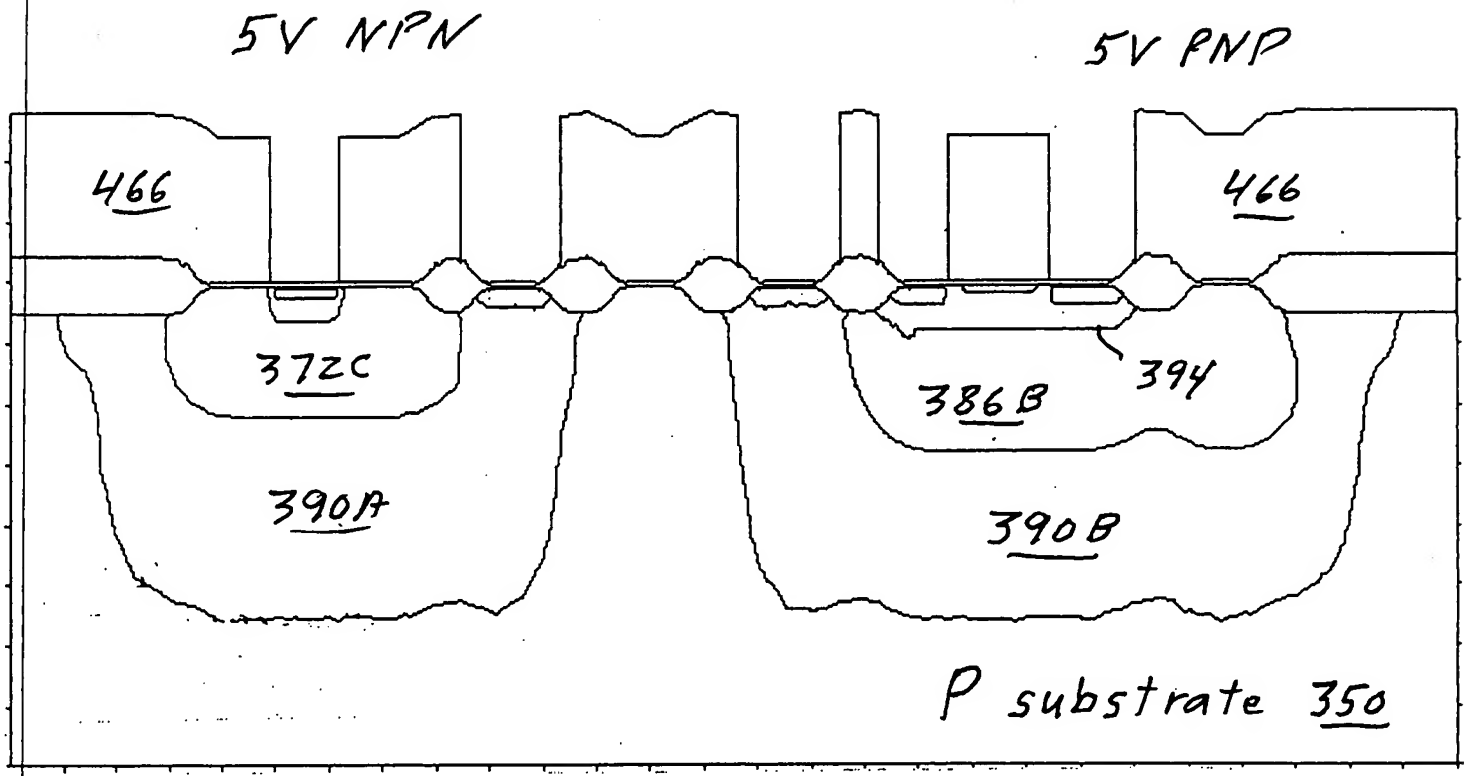
High F_T Layout



5V N-LDD Implant

Fig 6OB

Conventional Layout



5V N-LDD Implant

Fig. 60C

30V Lateral Trench DMOS 308

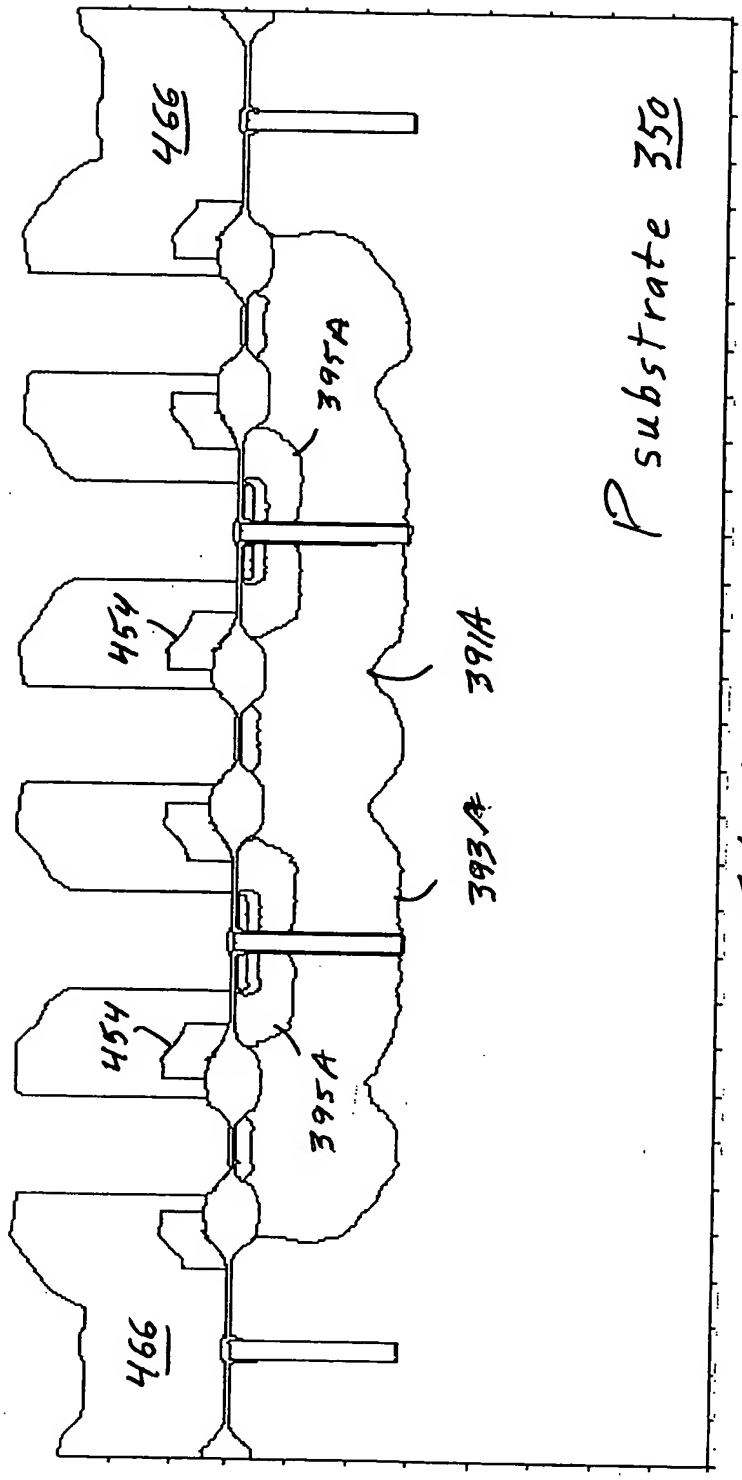


Fig. 6D

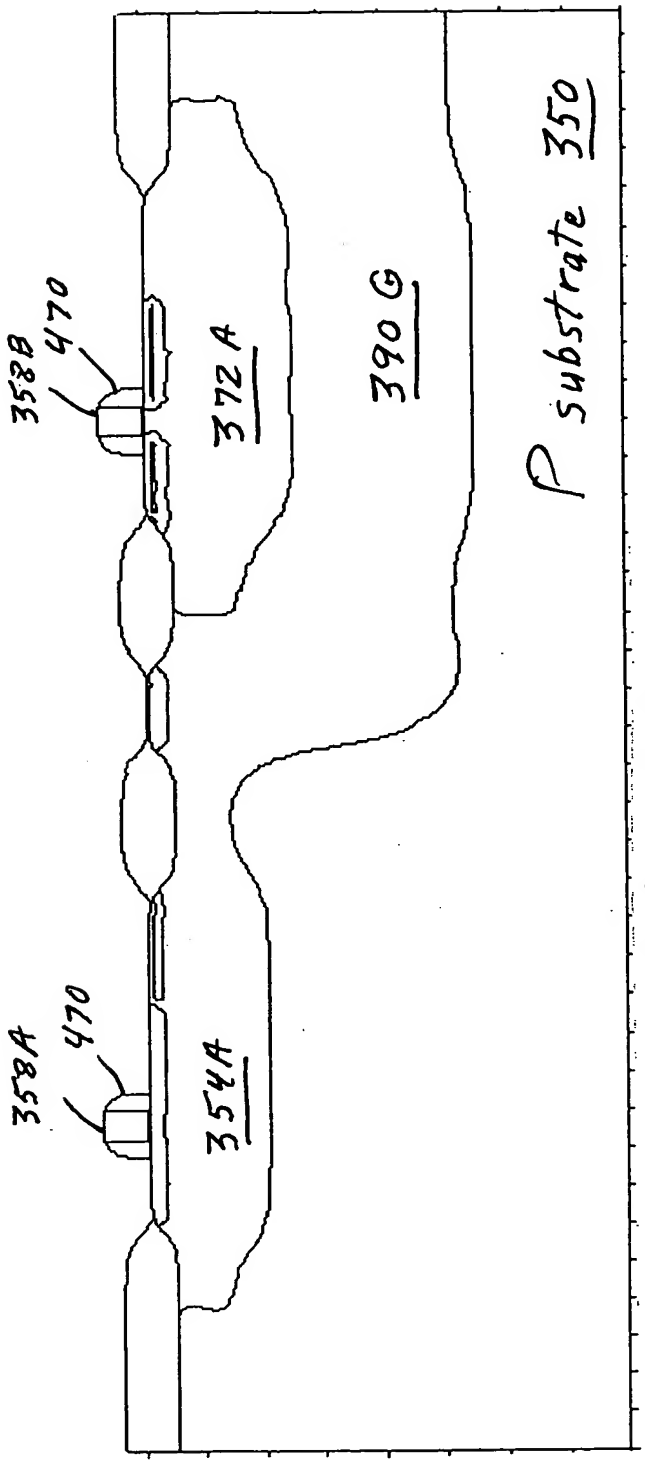

5V NMOS 302
5V PMOS 301
358B
470
372A
390G
P substrate 350
358A
470
354A
Sidewall Spacers

Fig. 6A

30V Lateral Trench DMOS 308

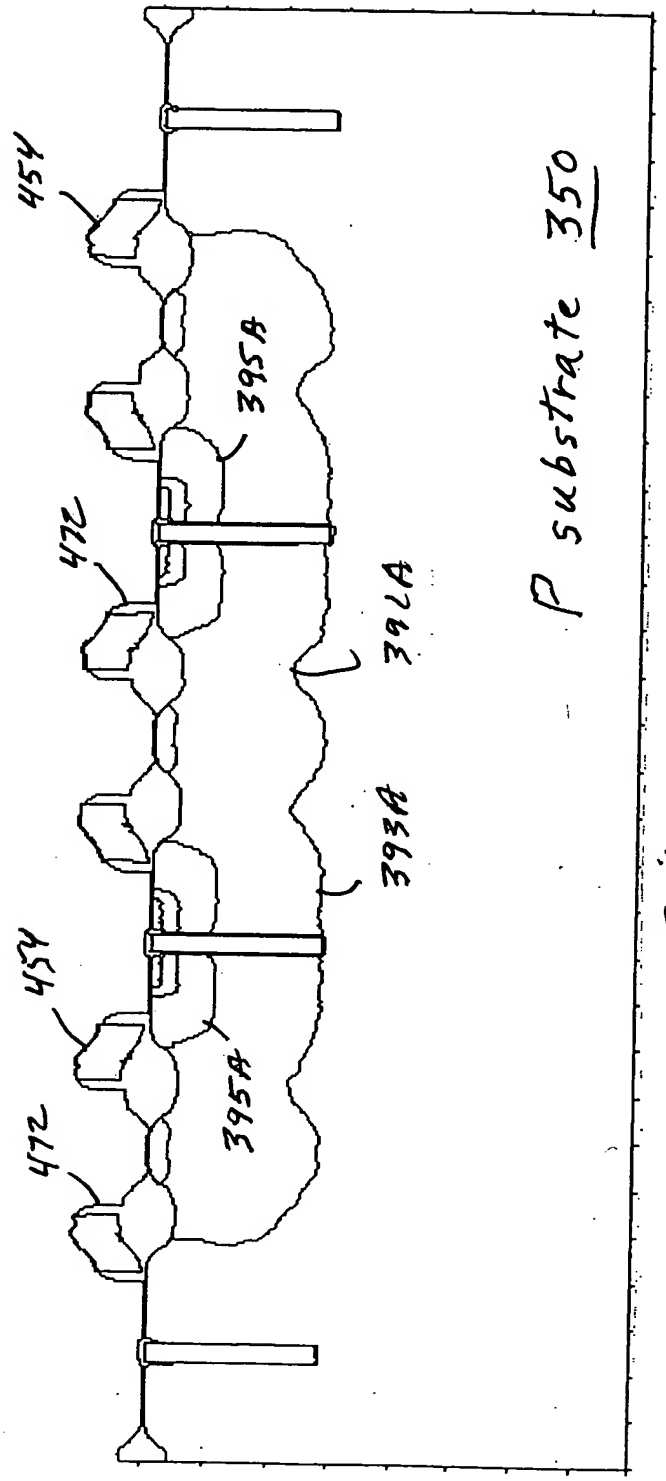


Fig. 61D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

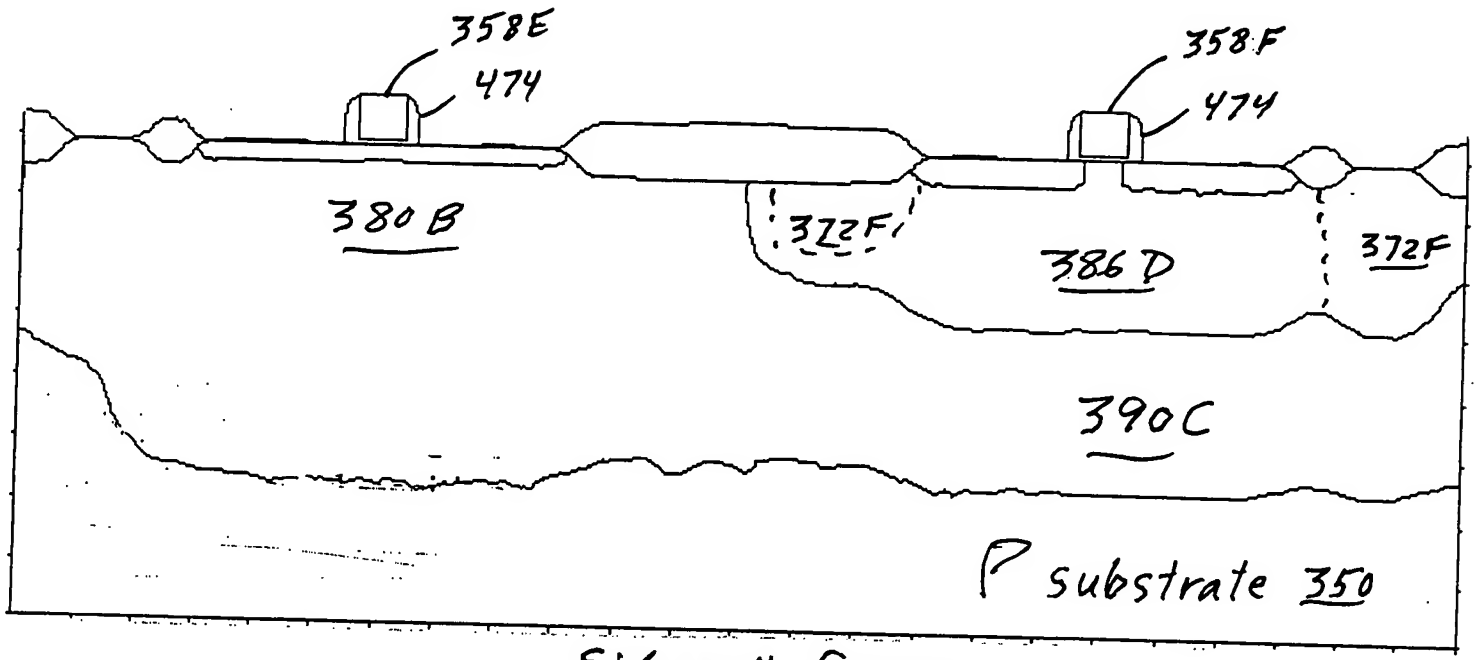
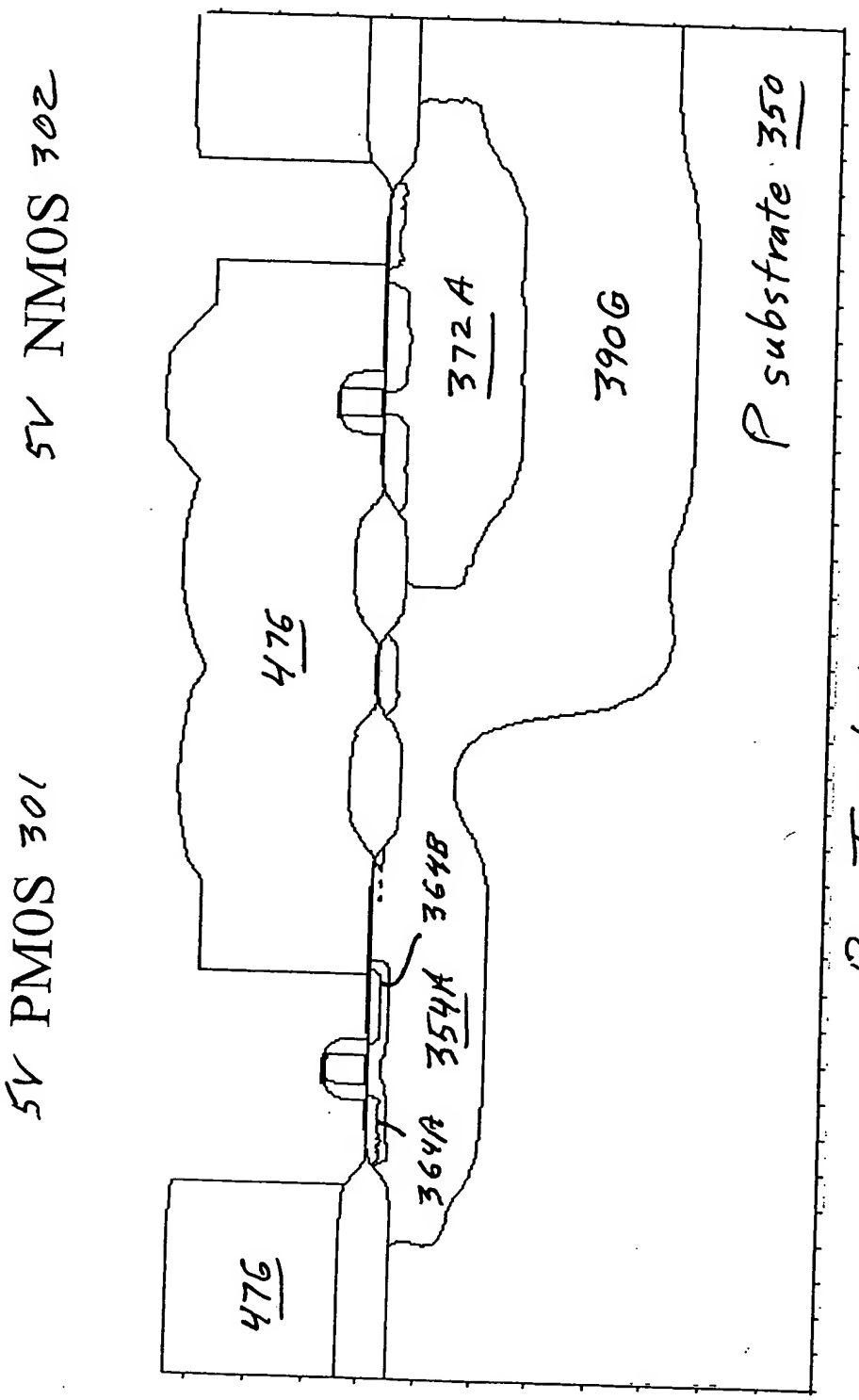


Fig. 61E


5V PMOS 301
5V NMOS 302
476
372A
390G
P substrate 350
364B
354A
364A
476
P+ Implant
Fig. 62A

High F_T Layout

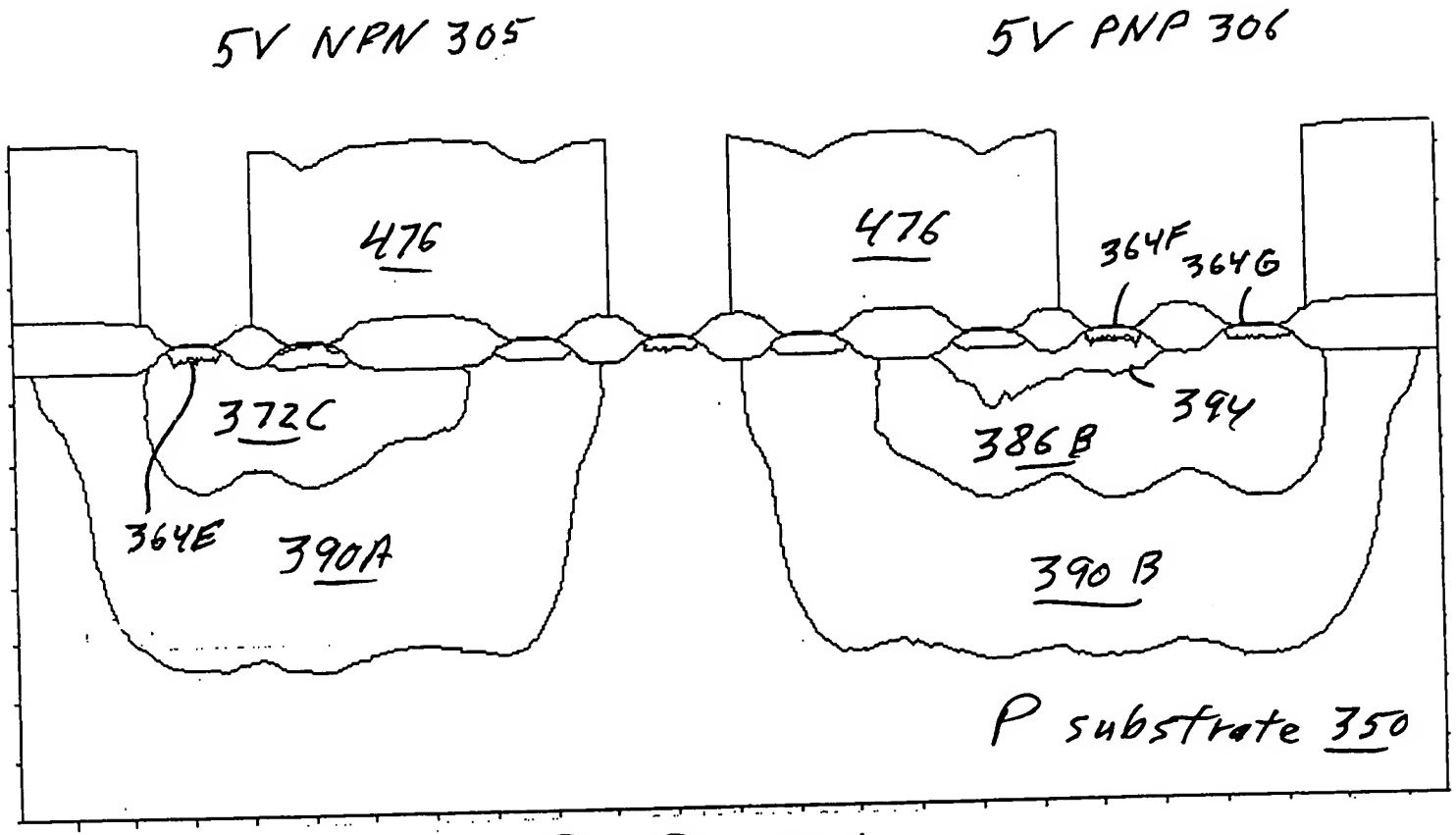
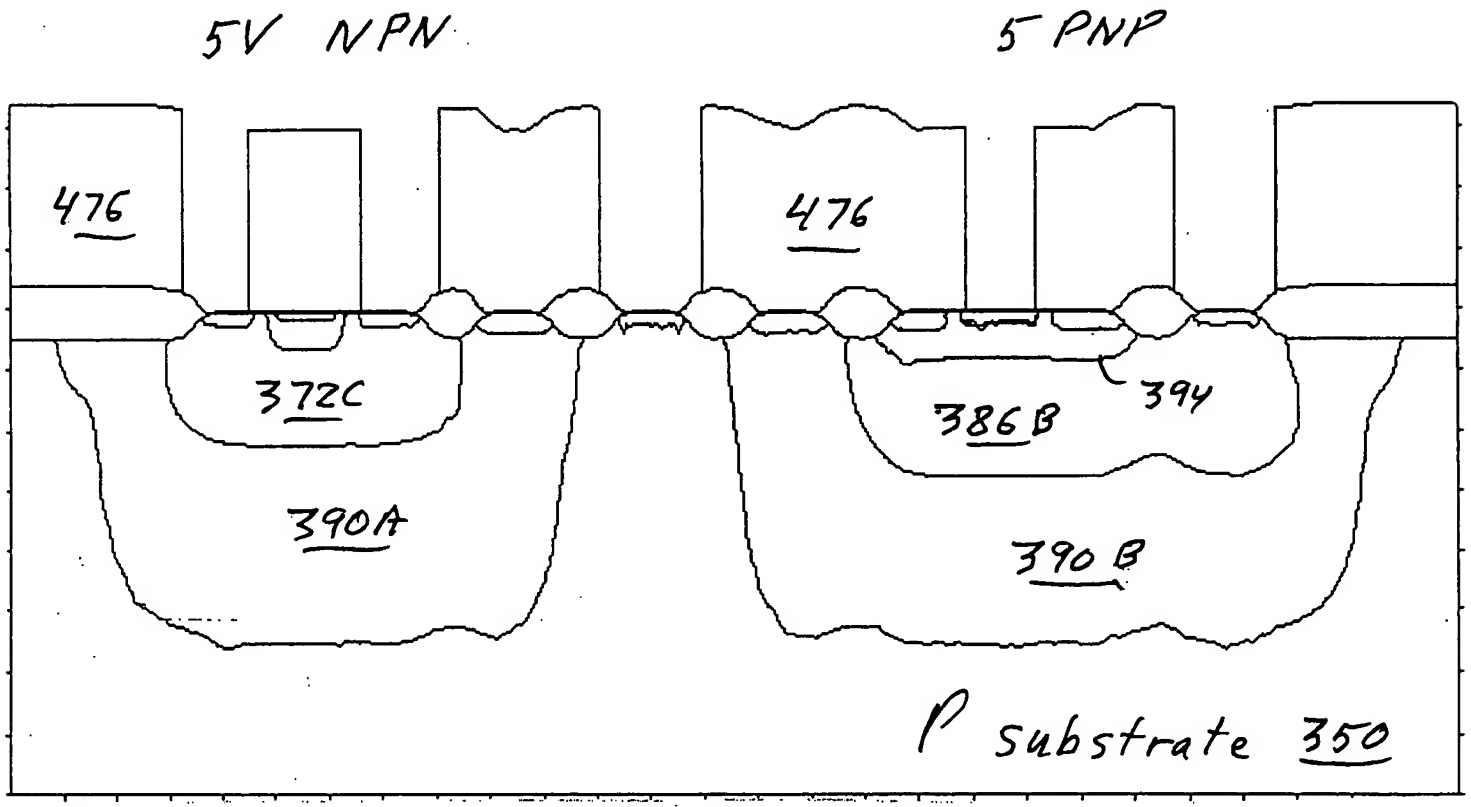


Fig. 62B

Conventional Layout



P+ Implant

Fig. 62C

30V Lateral Trench DMOS 308

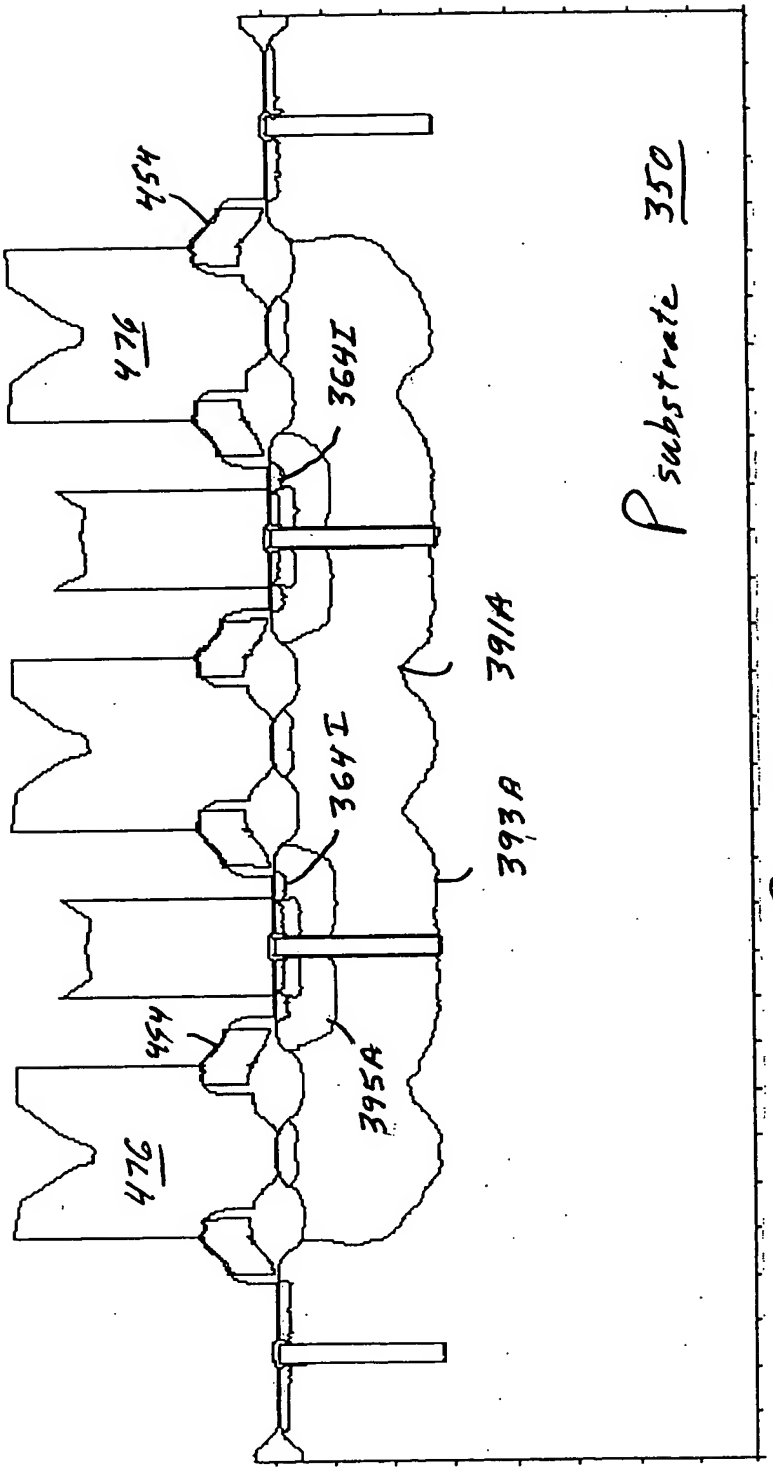
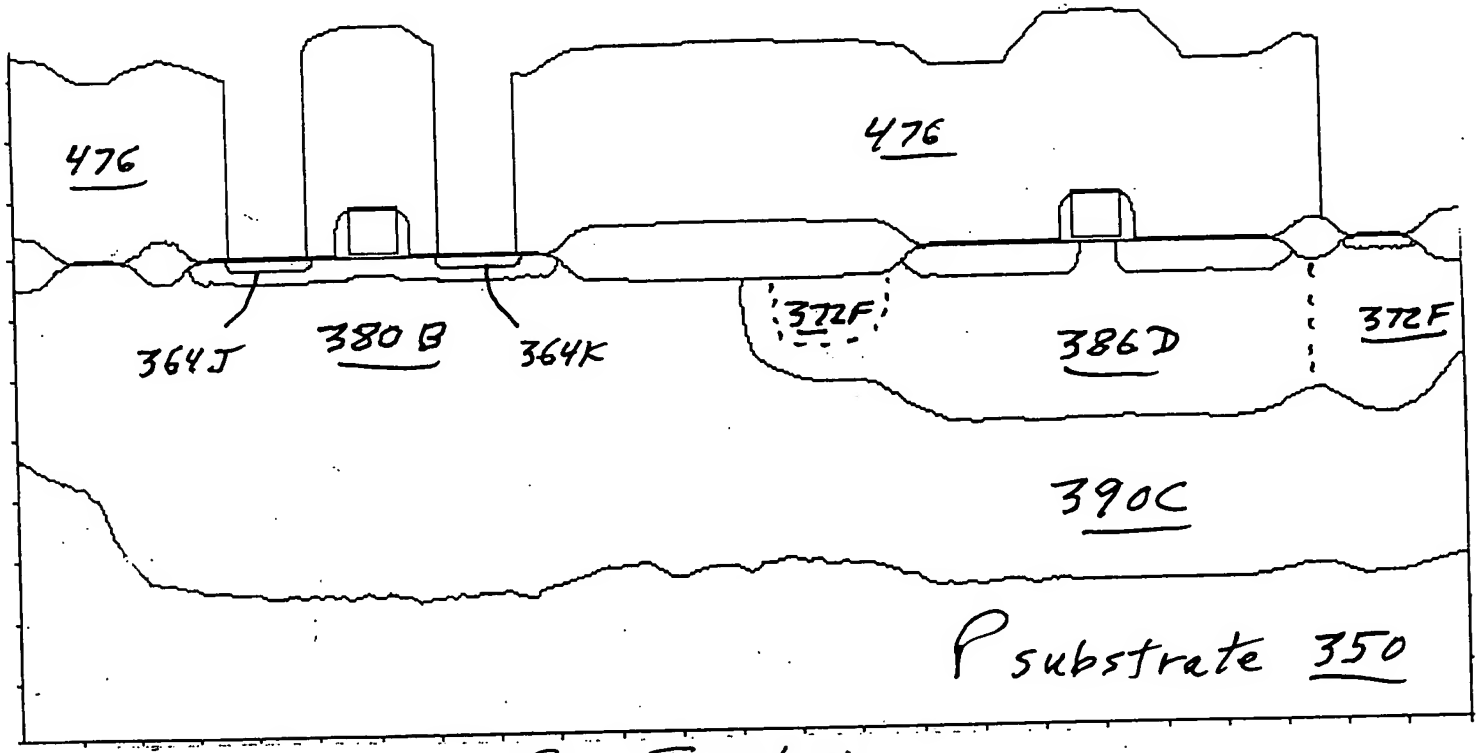


Fig. 62D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310

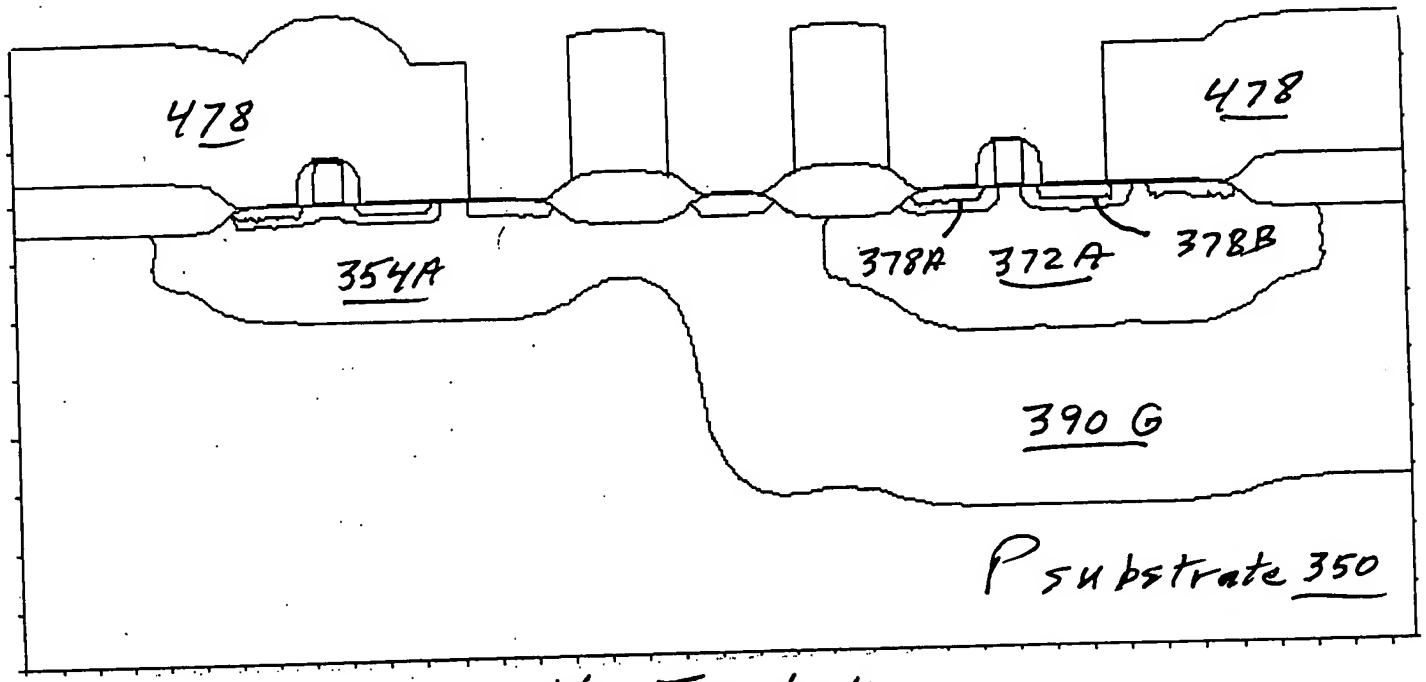


P+ Implant

Fig 62E

5V PMOS 301

5V NMOS 302



N+ Implant

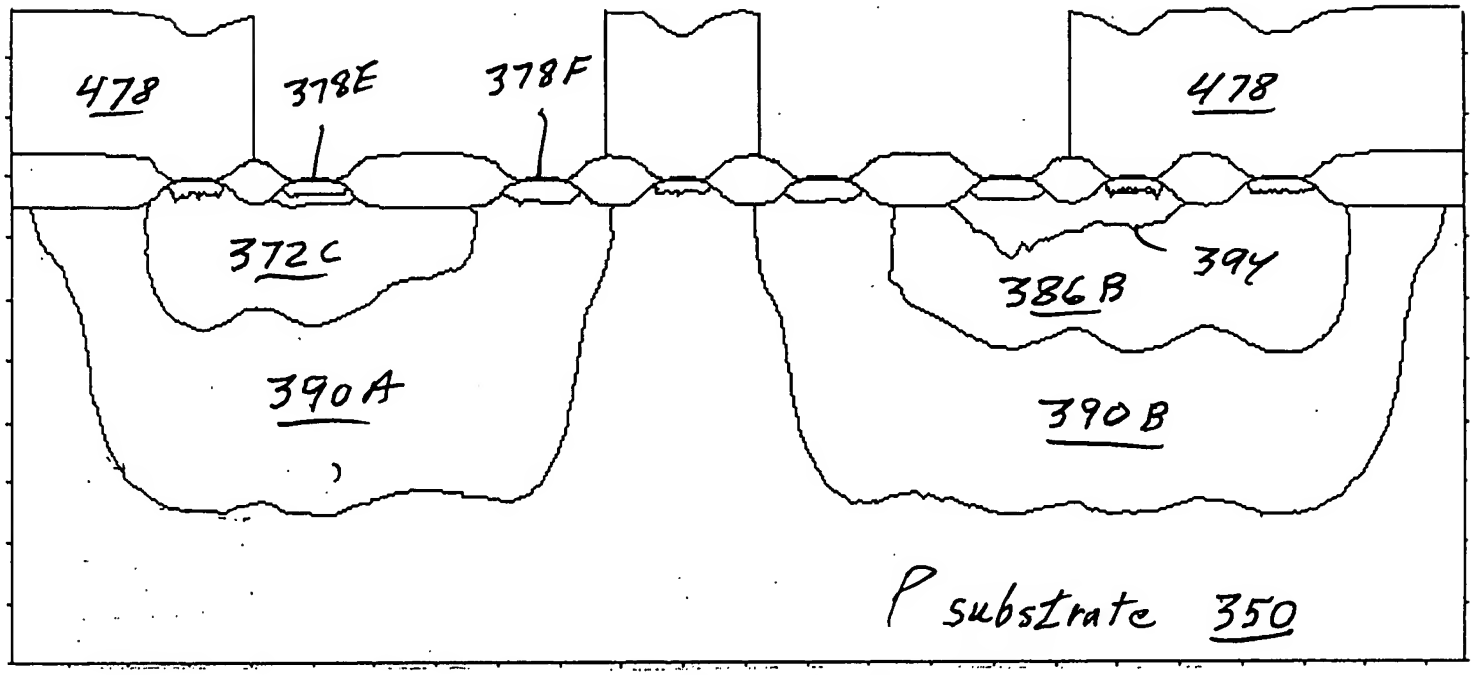
Fig. 63A

6/2/06

High F_T Layout

5V NPN 305

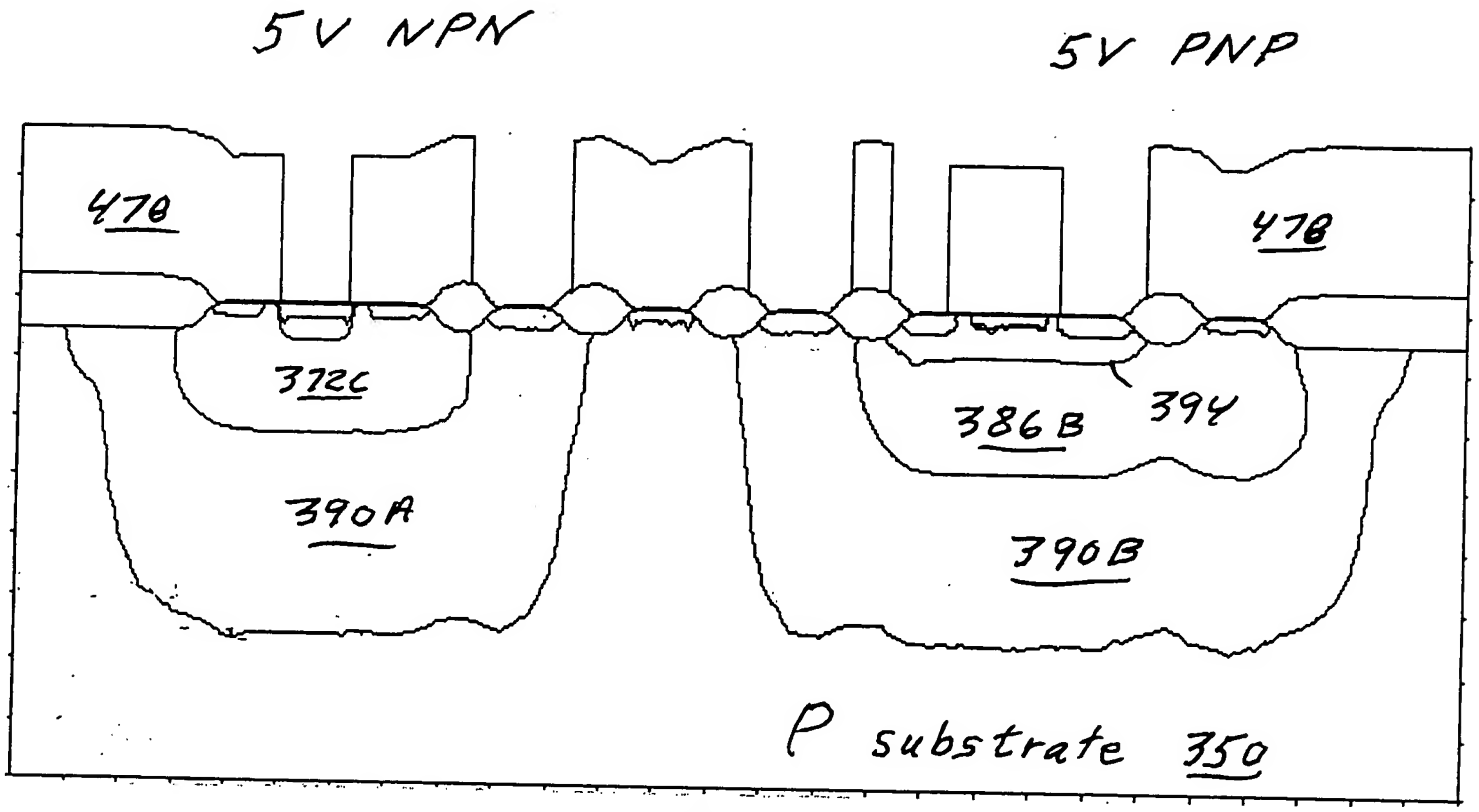
5V PNP 306



N+ Implant

Fig. 63B

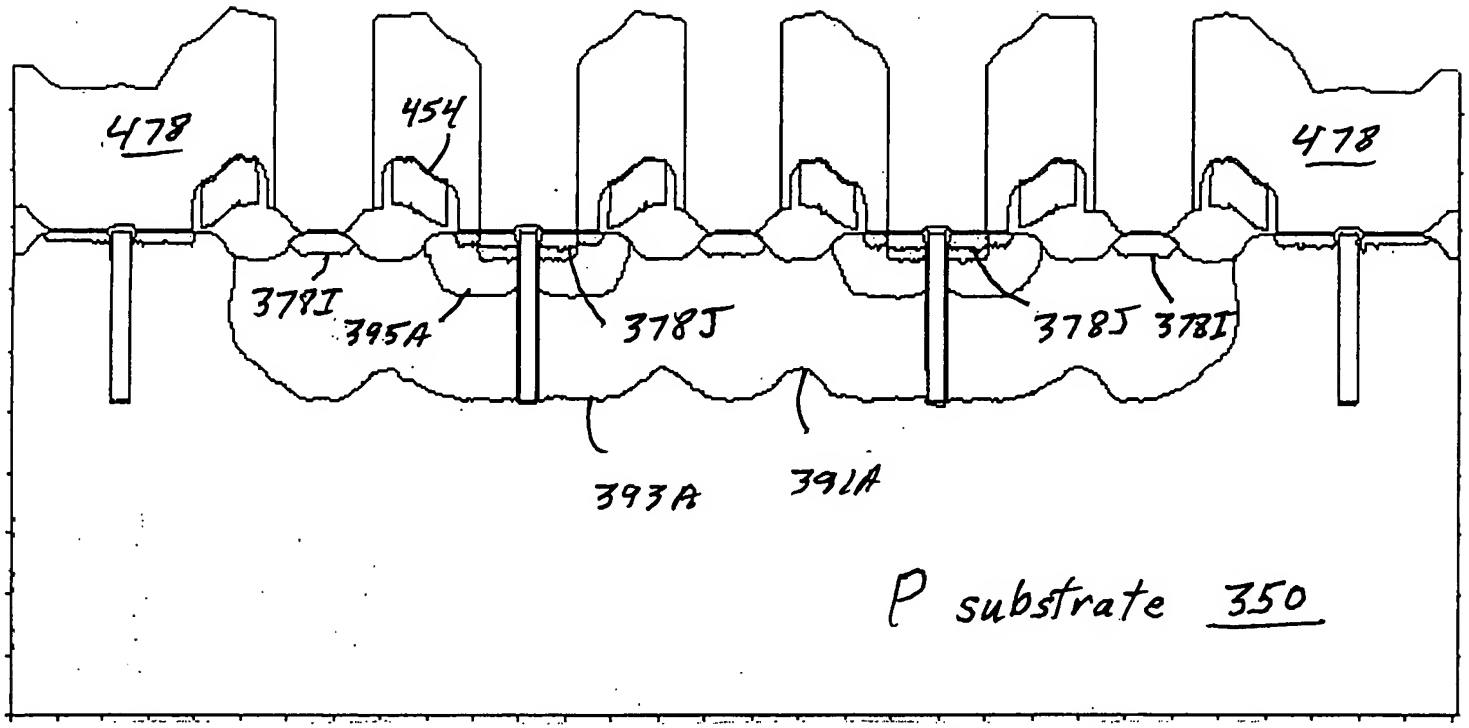
Conventional Layout



Nt Implant

Fig. 63C

30V Lateral Trench DMOS 308

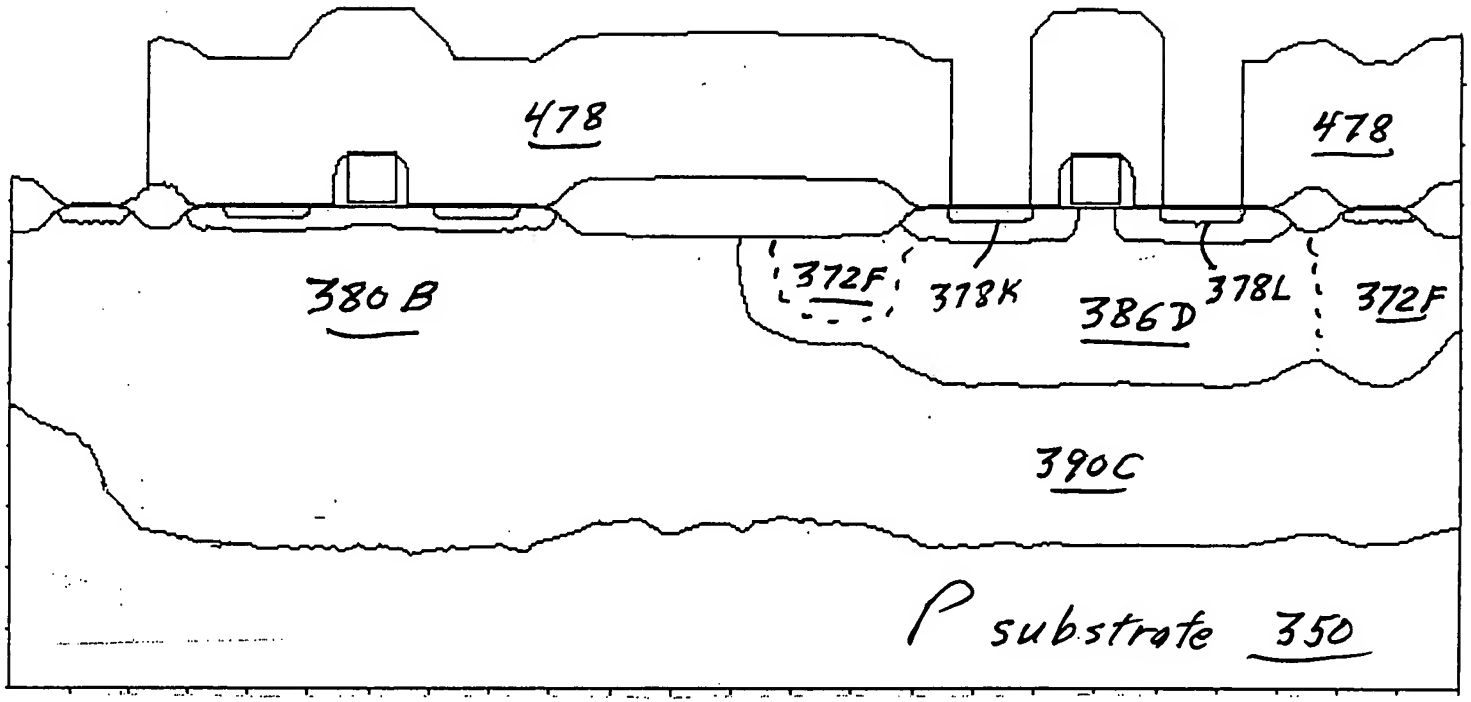


N+ Implant

Fig 63D

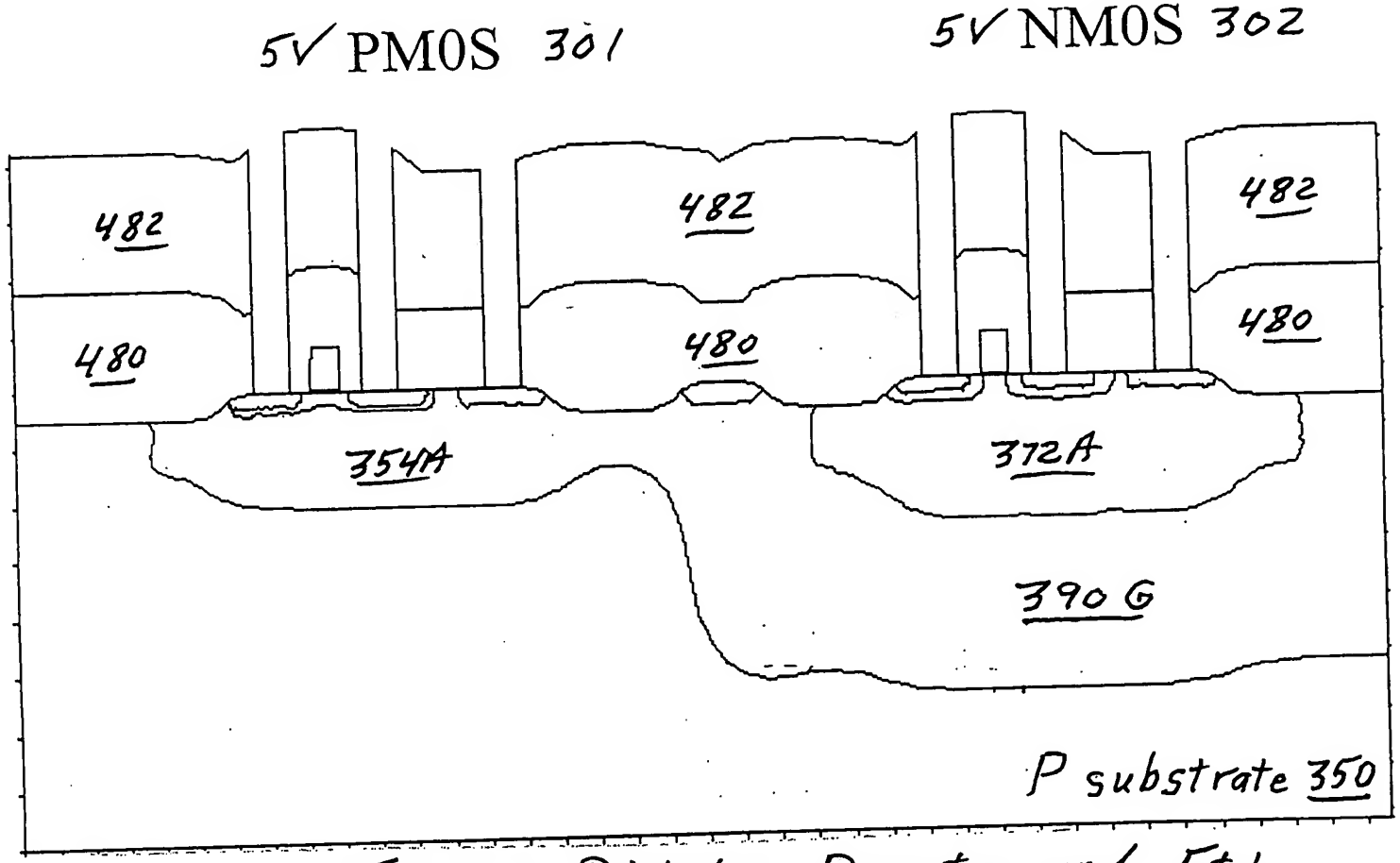
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



N+ Implant

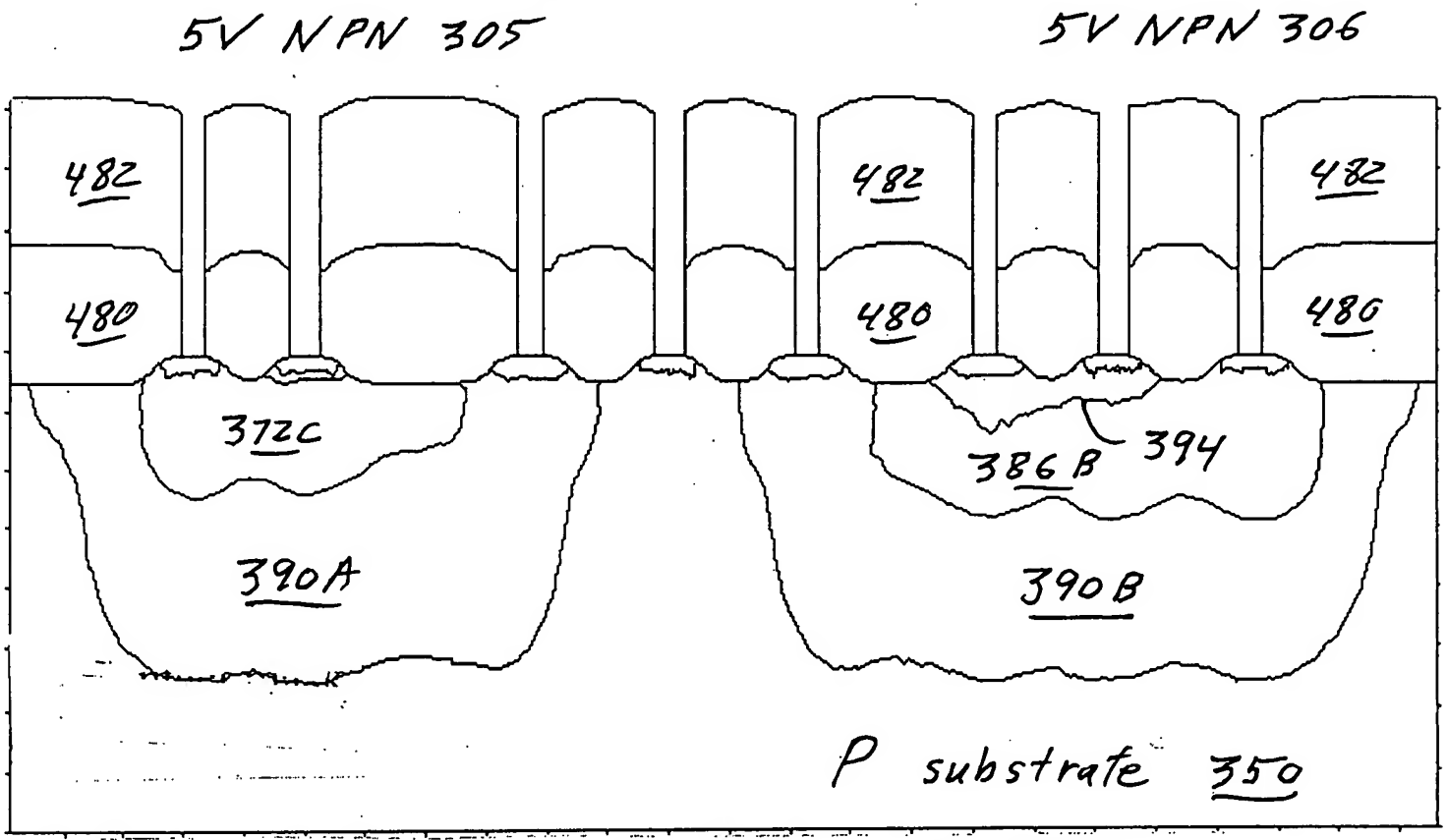
Fig 63E



Interlayer Dielectric Deposition and Etch

Fig. 64A

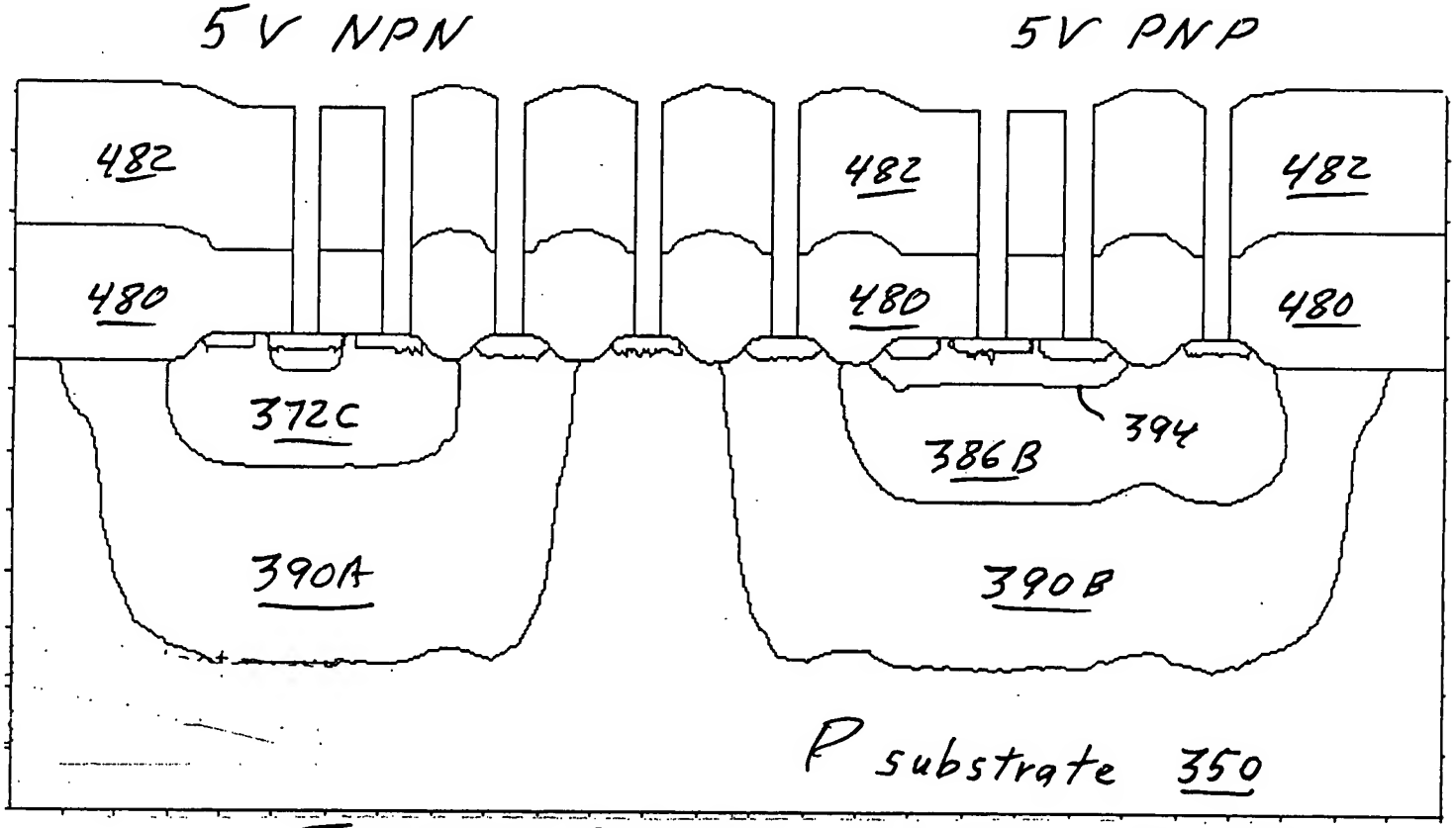
High F_T Layout



Interlayer Dielectric Deposition and Etch

Fig. 64B

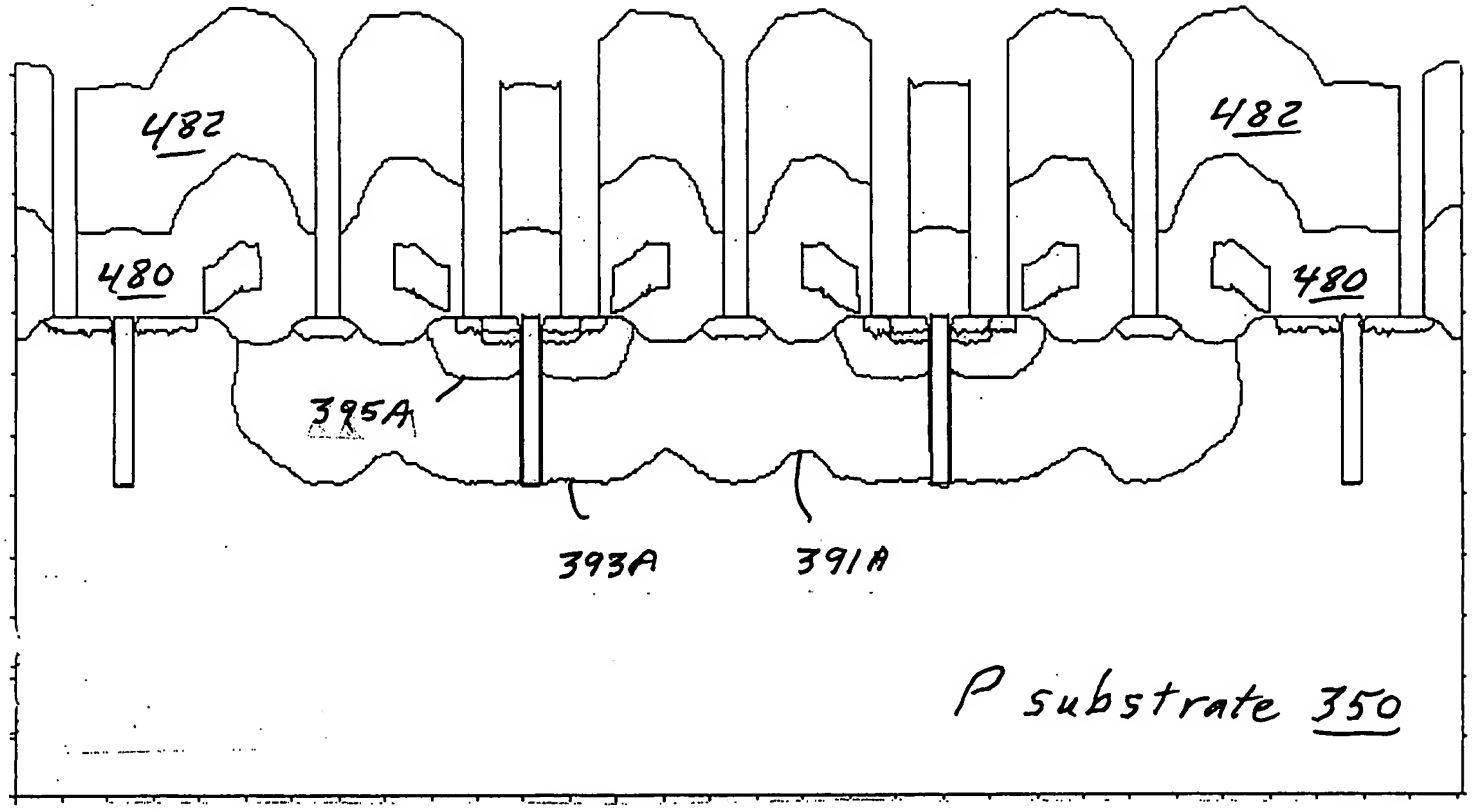
Conventional Layout



Interlayer Dielectric Deposition and Etch

Fig. 64C

30V Lateral Trench DMOS 308

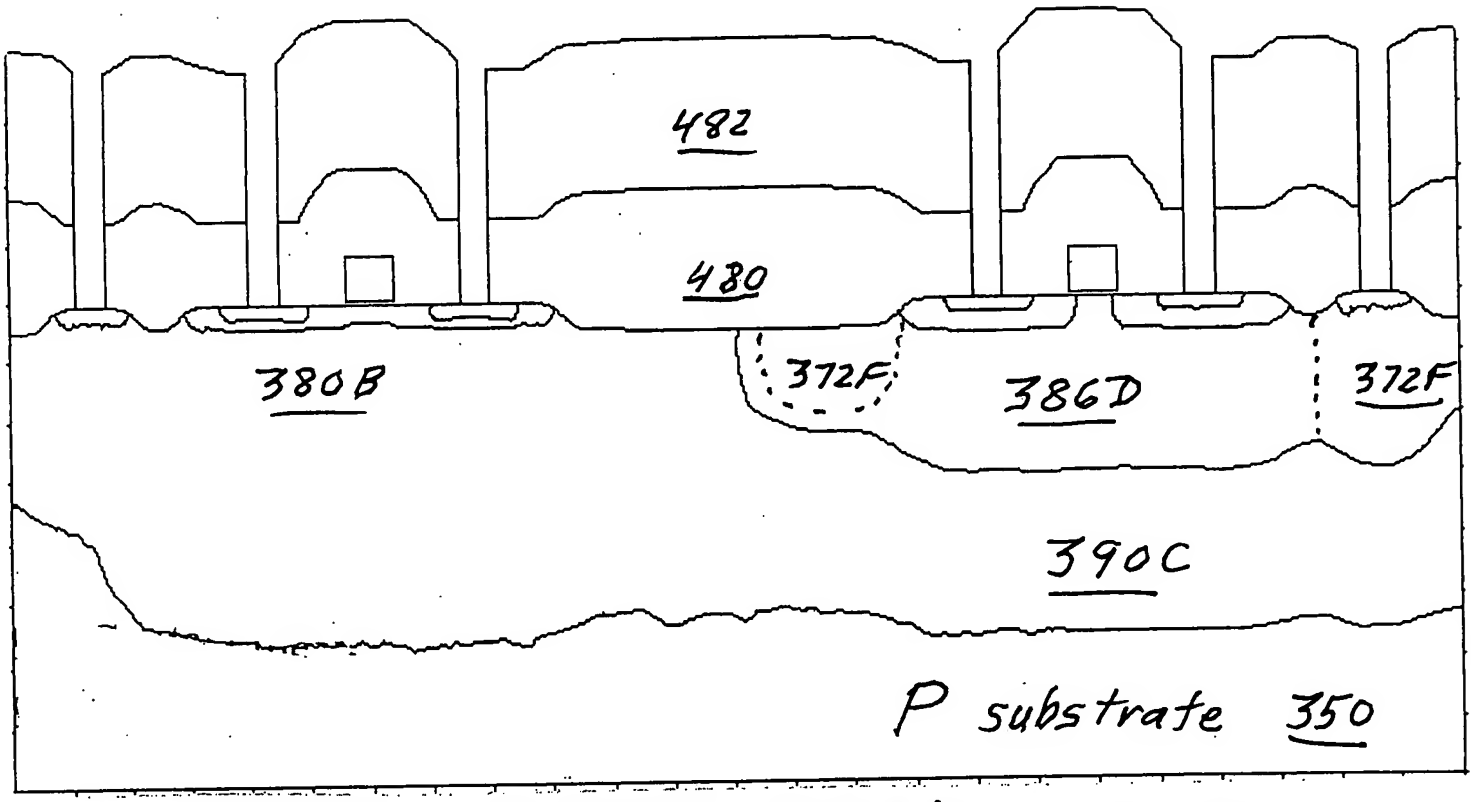


Interlayer Dielectric Deposition and Etch

Fig. 6D

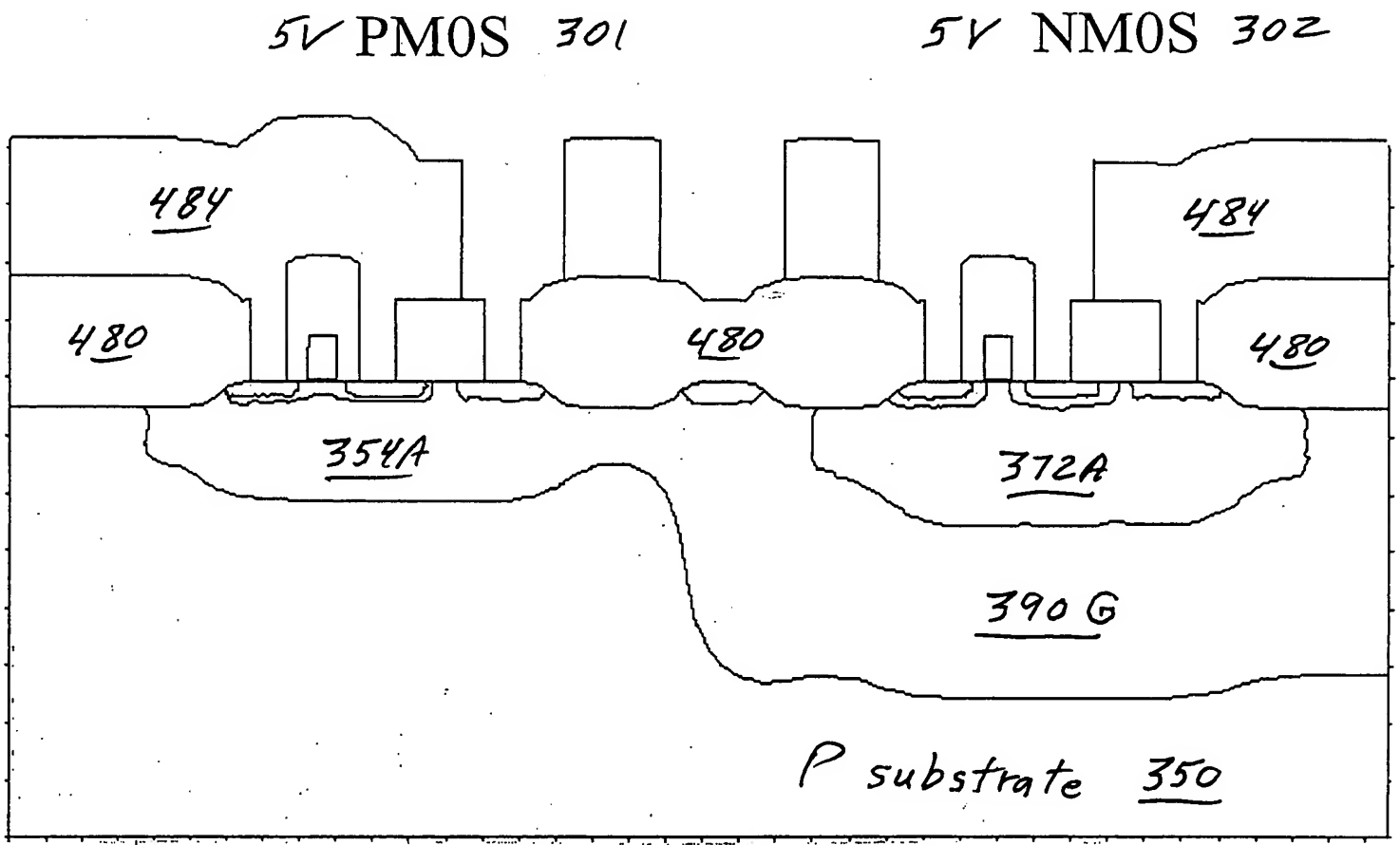
Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Interlayer Dielectric Deposition and Etch

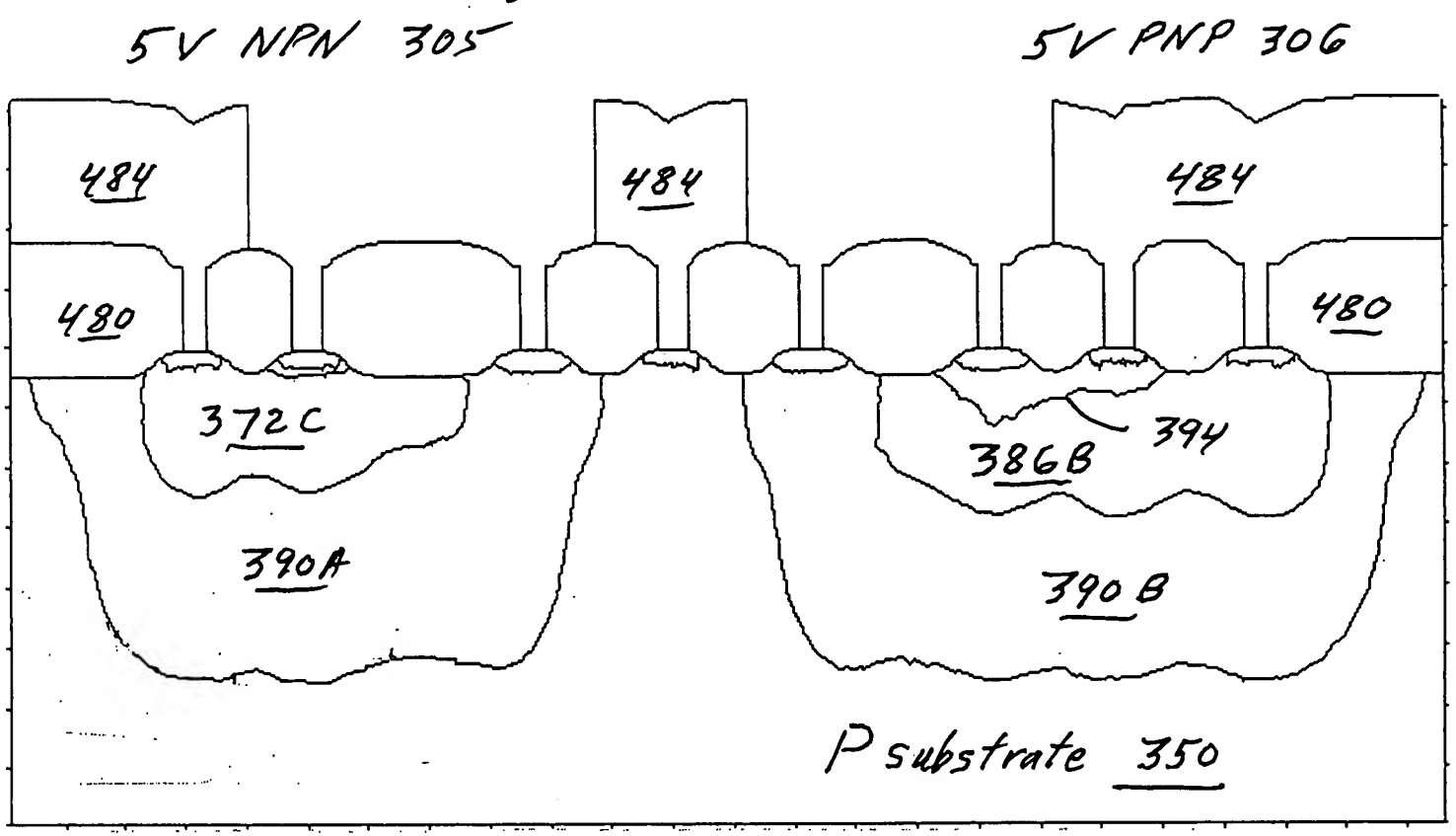
Fig 64E



N-plug Mask and Implant

Fig. 65A

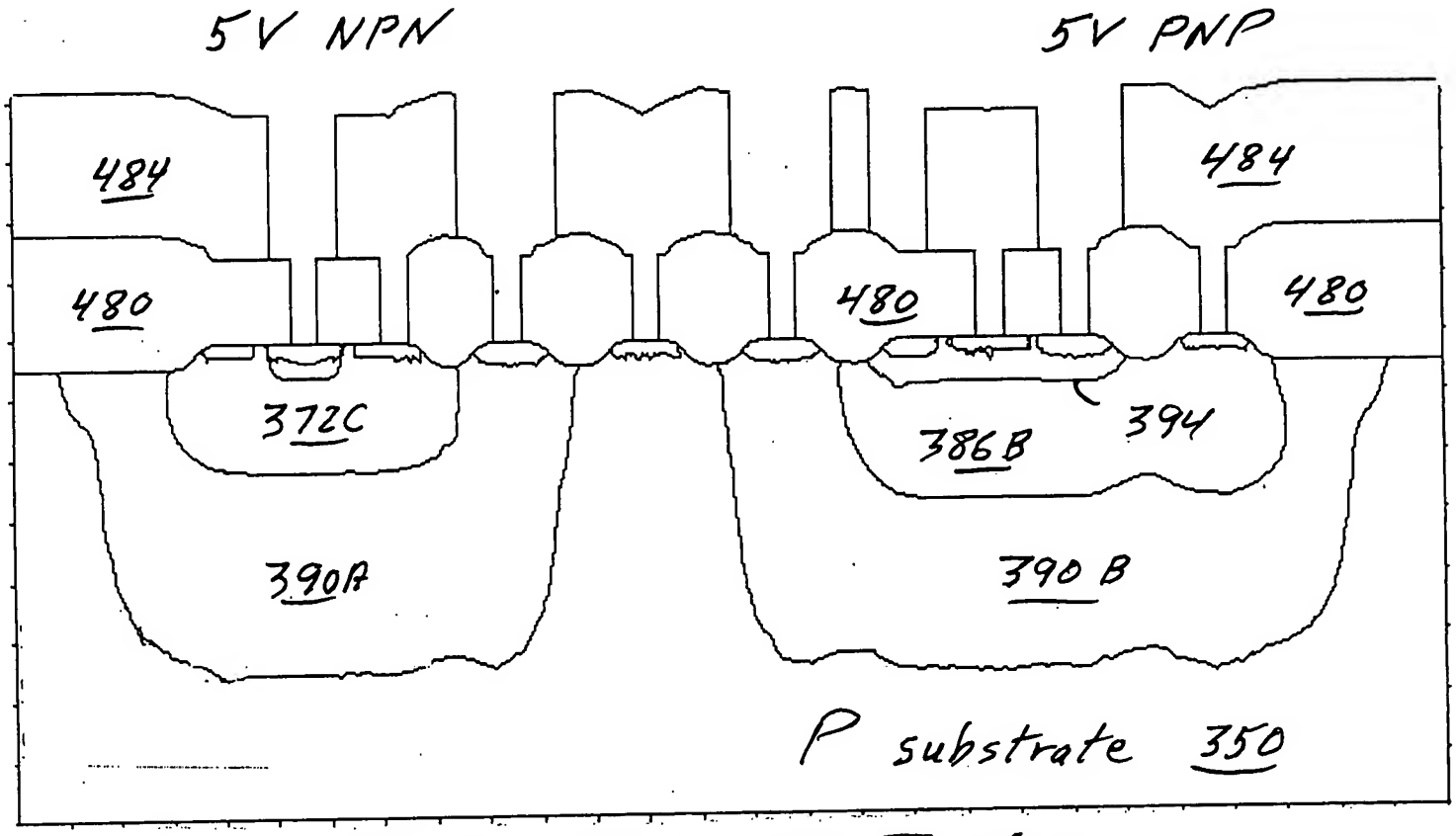
High F_T Layout



N-plug Mask and Implant

Fig 6SB

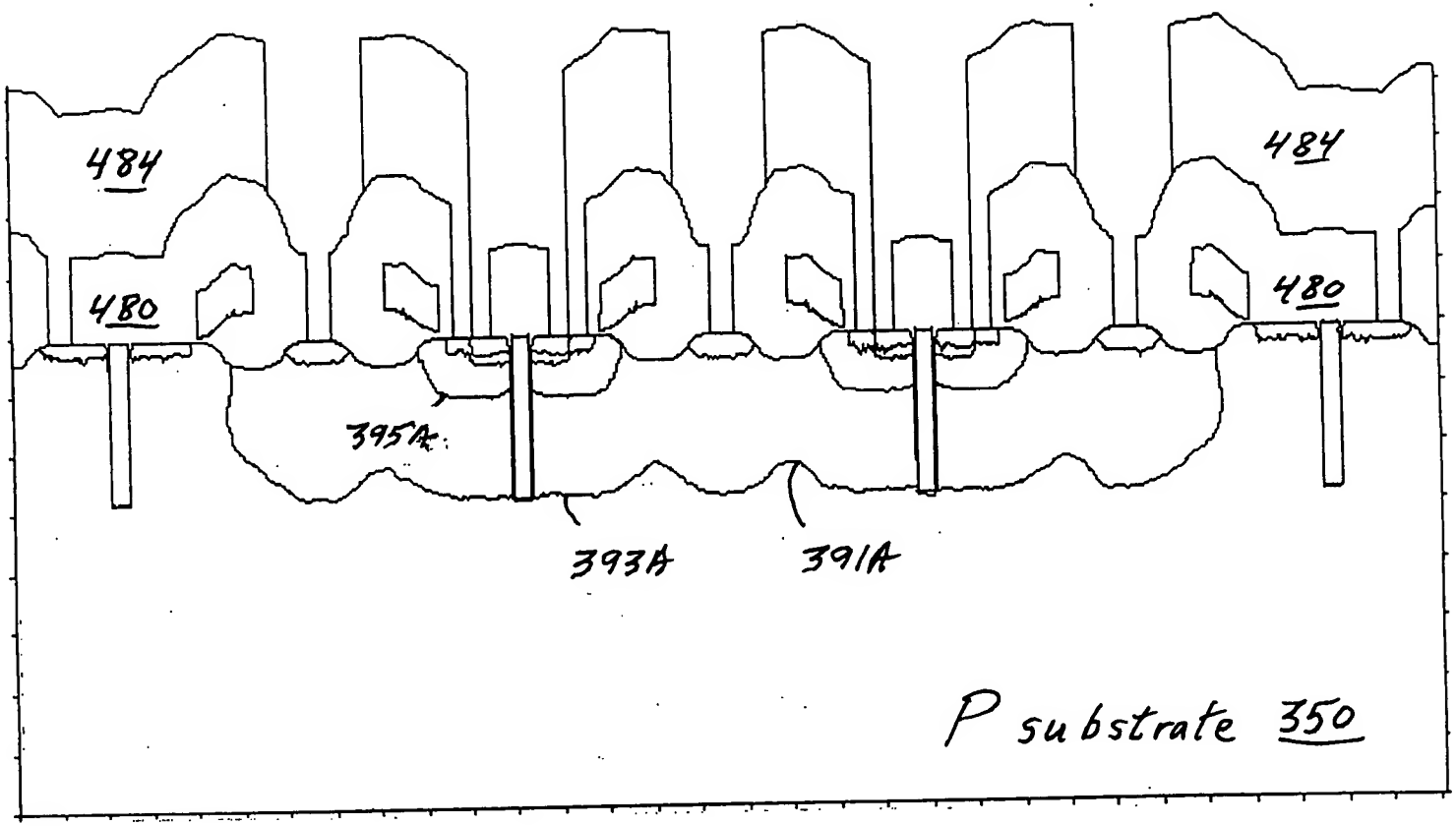
Conventional Layout



N-plug Mask and Implant

Fig. 6S C

30V Lateral Trench DMOS 308

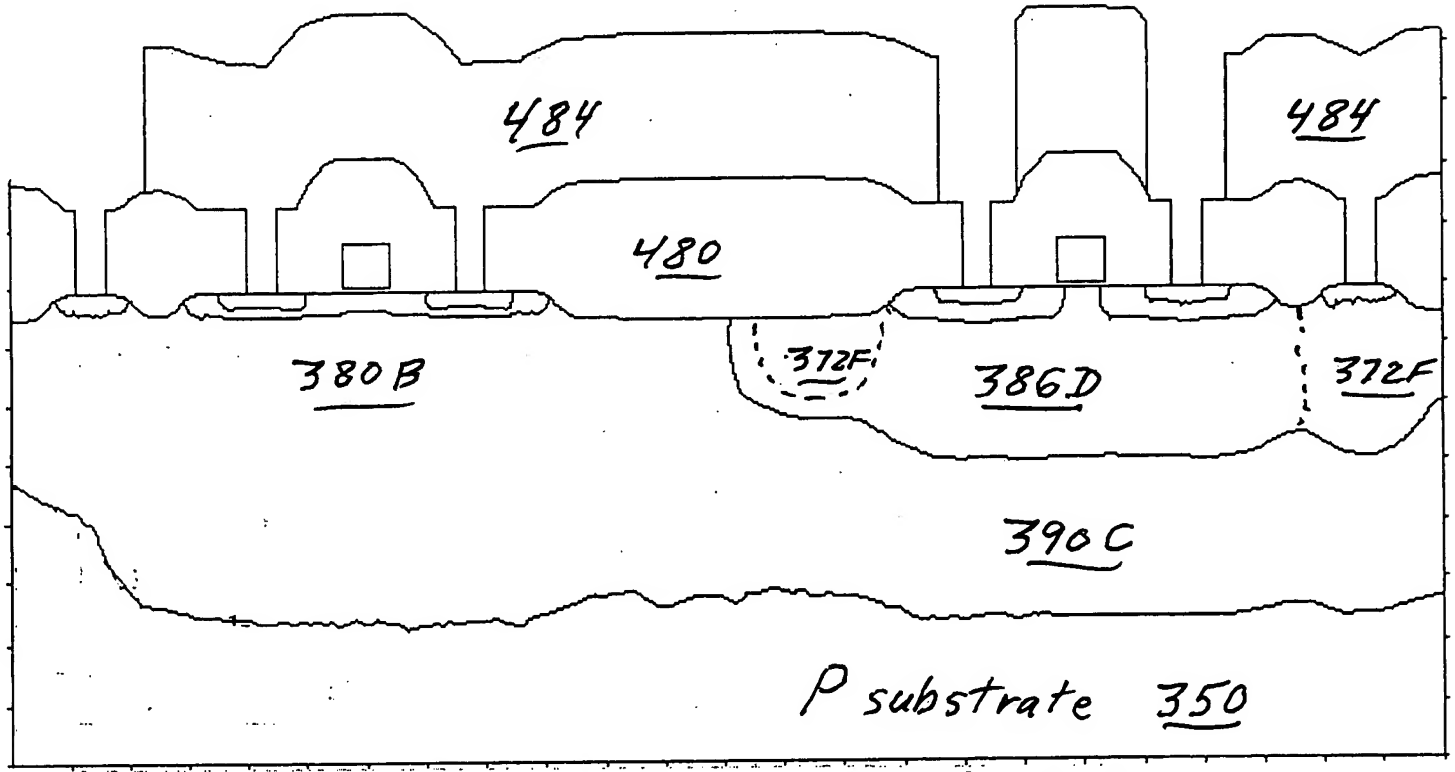


N-plug Mask and Implant

Fig 65D

Symmetrical 12V CMOS

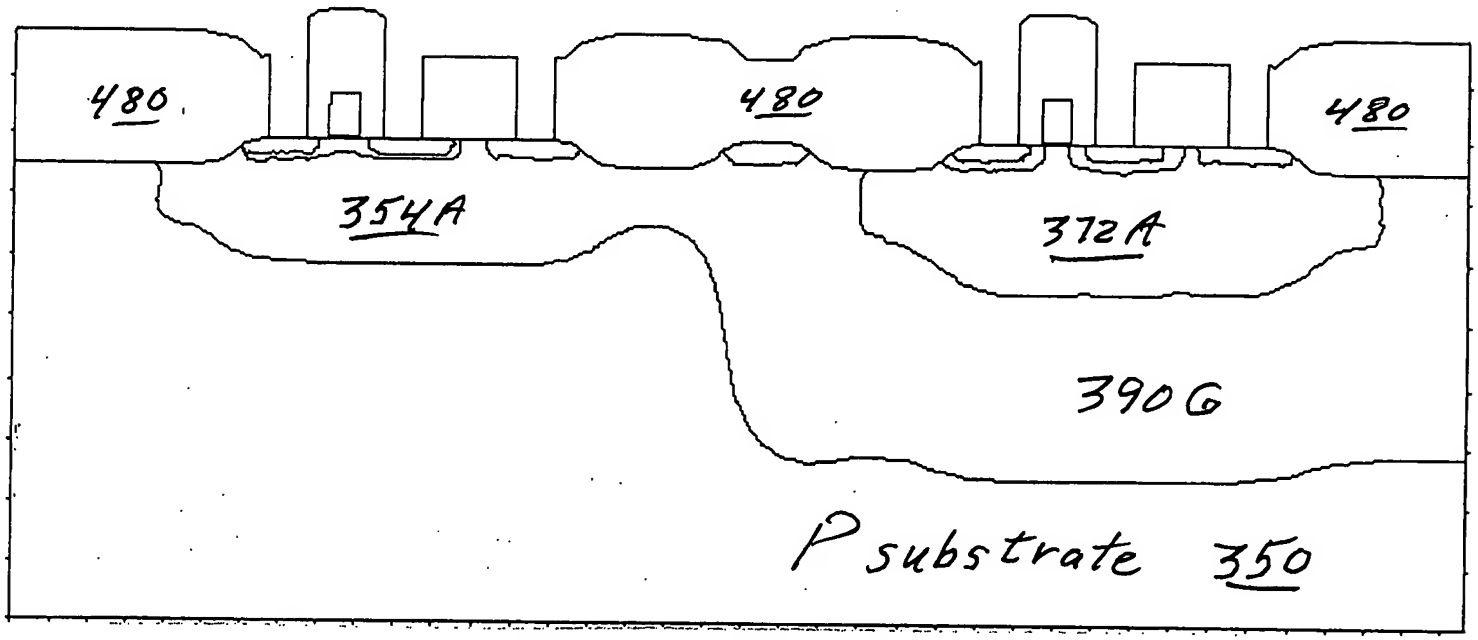
12V PMOS 309 12V NMOS 310



N-plug Mask and Implant

Fig 65E

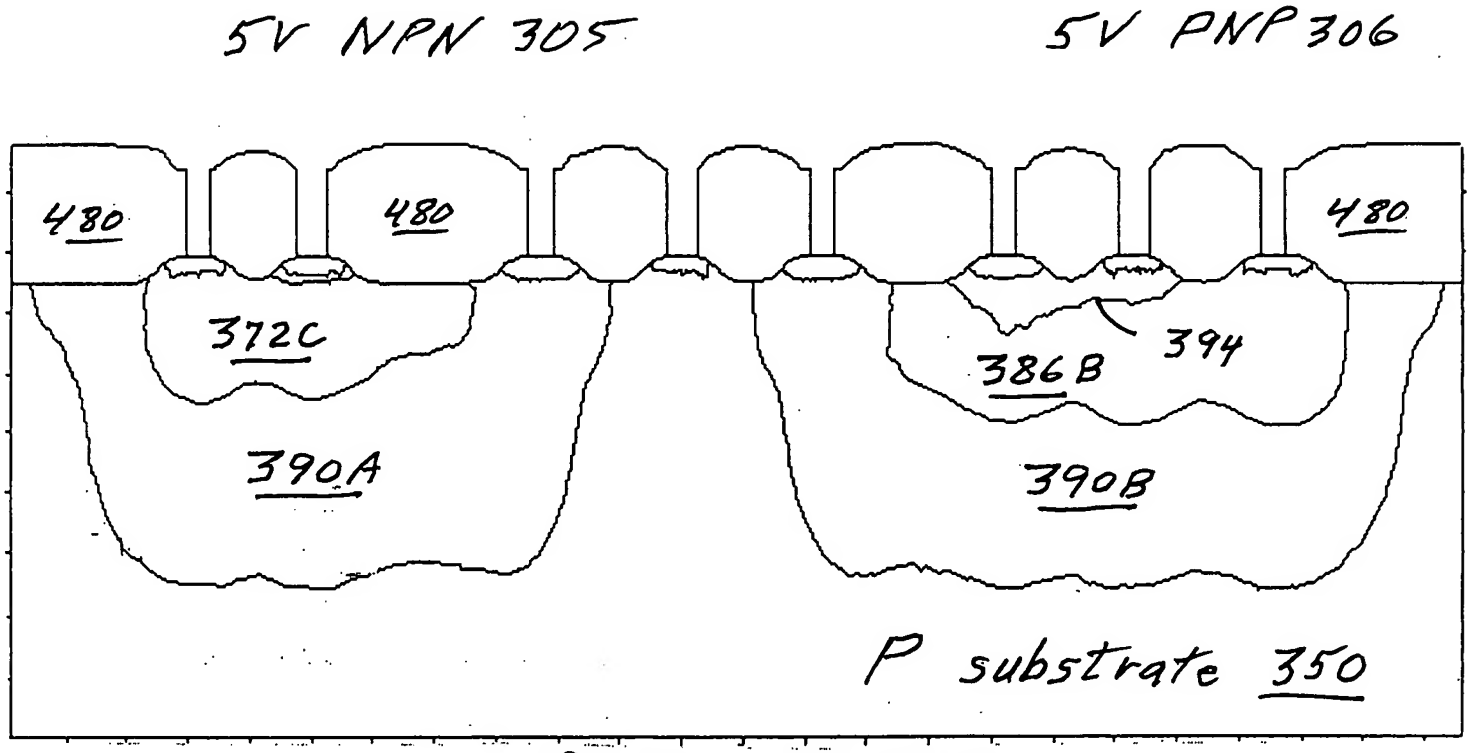
5V PMOS 301 5V NMOS 302



P-plug Implant

Fig. 66A

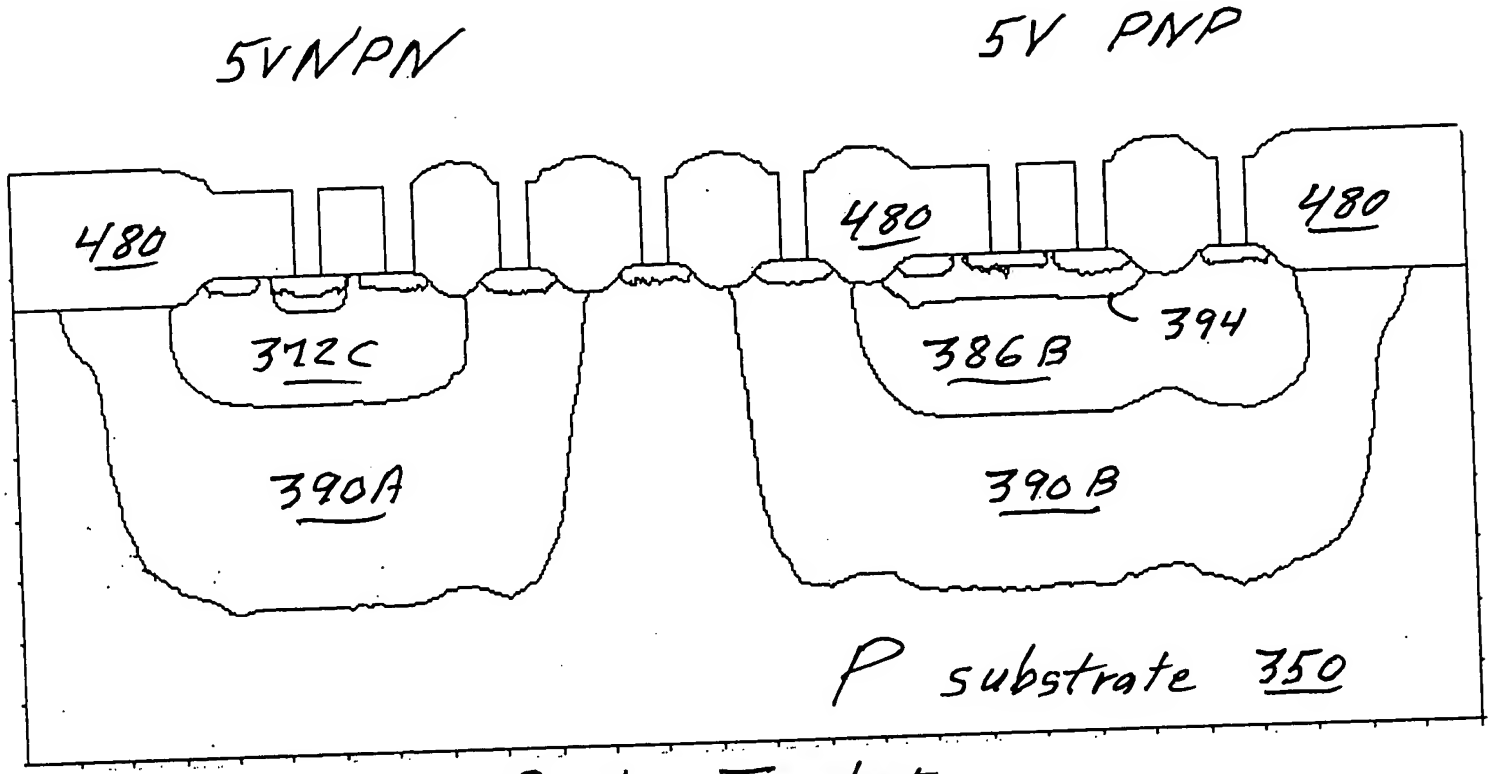
High F_T Layout



P-plug Implant

Fig. 6B

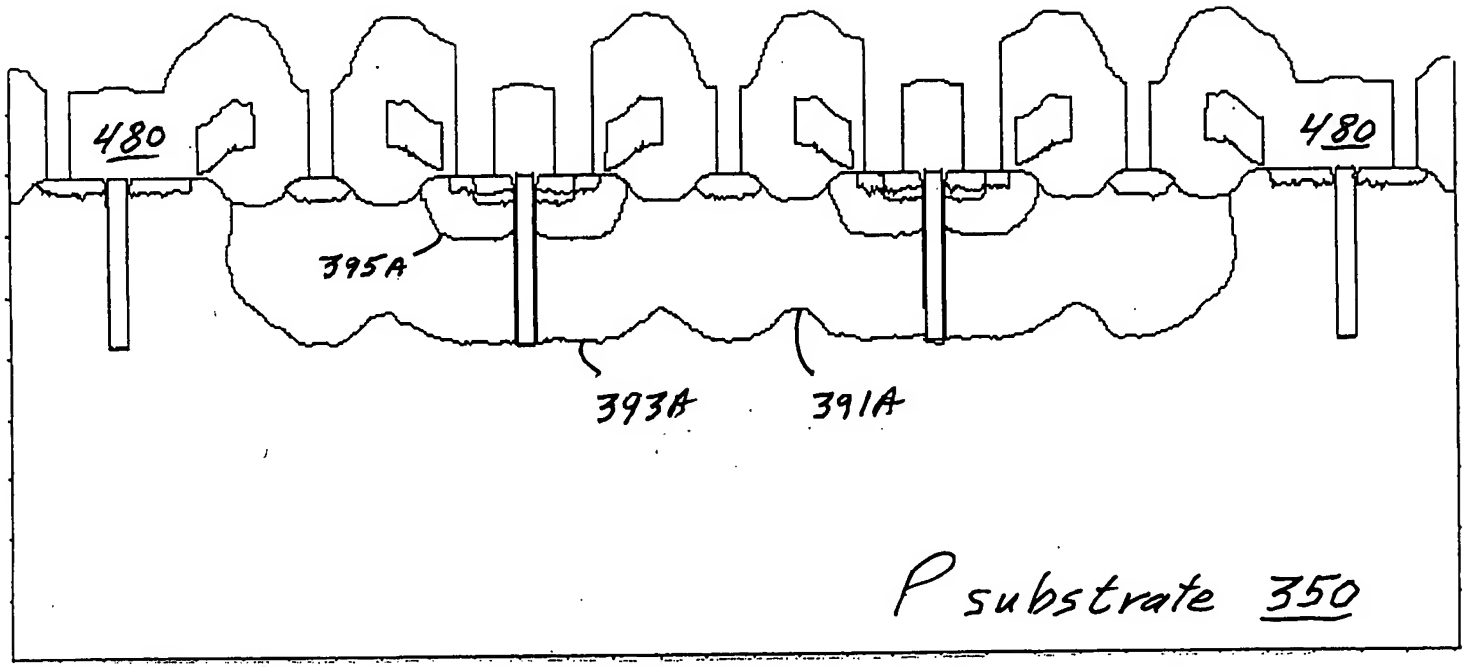
Conventional Layout



P-plug Implant
Fig. 66C

612/402

30V Latera / Trench DMOS 308

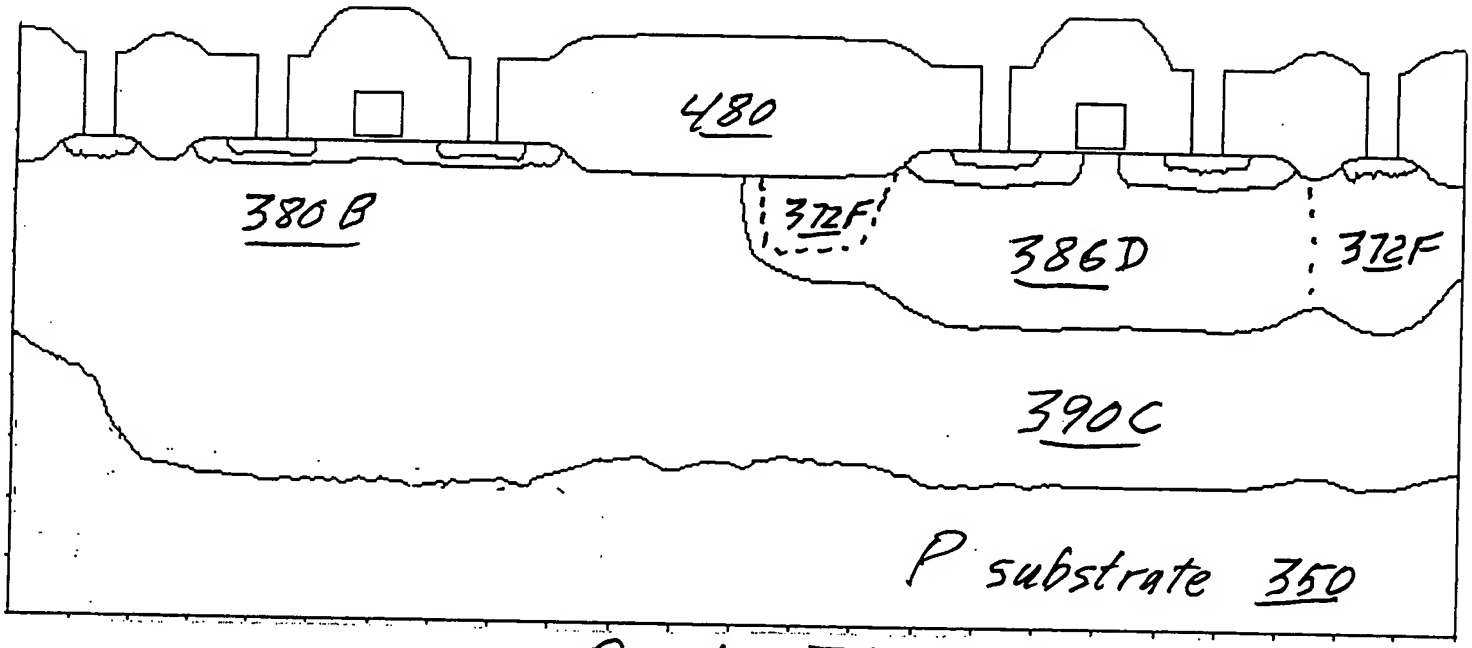


P-plug Implant

Fig 66D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



P-plug Implant

Fig. 66E

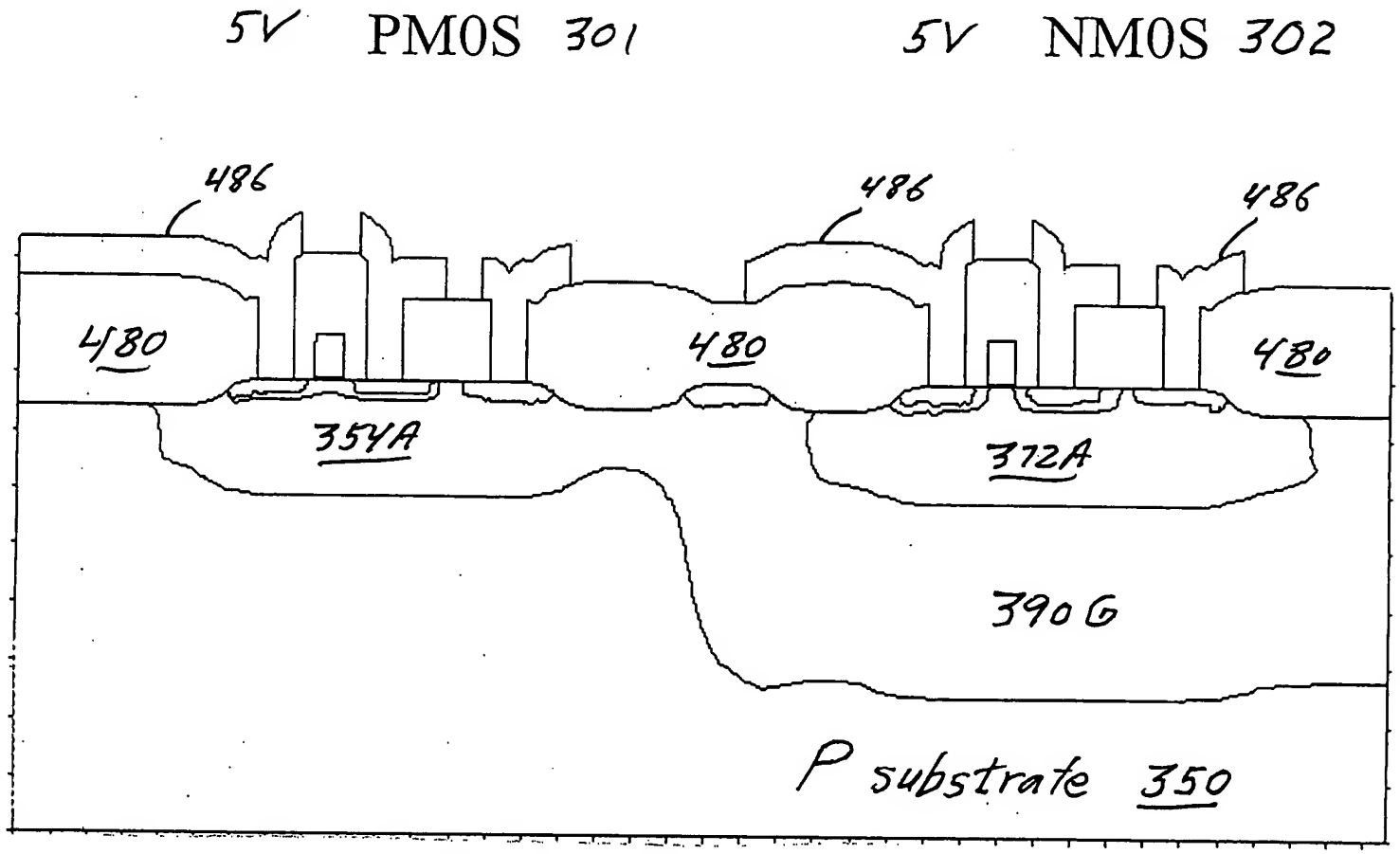

5V PMOS 301
5V NMOS 302
486
486
486
480
480
480
354A
372A
390G
P substrate 350
Metal Layer

Fig. 6A

High F_T Layout

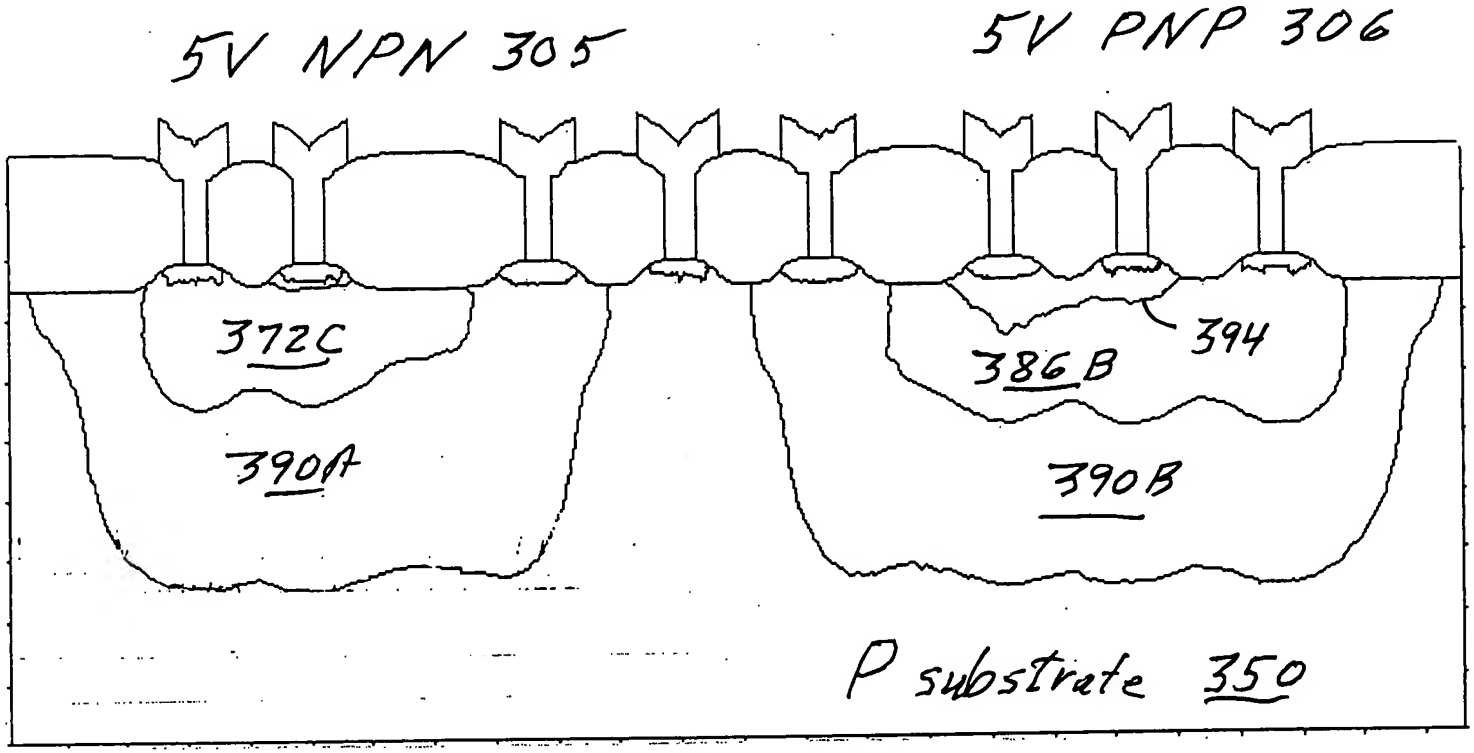
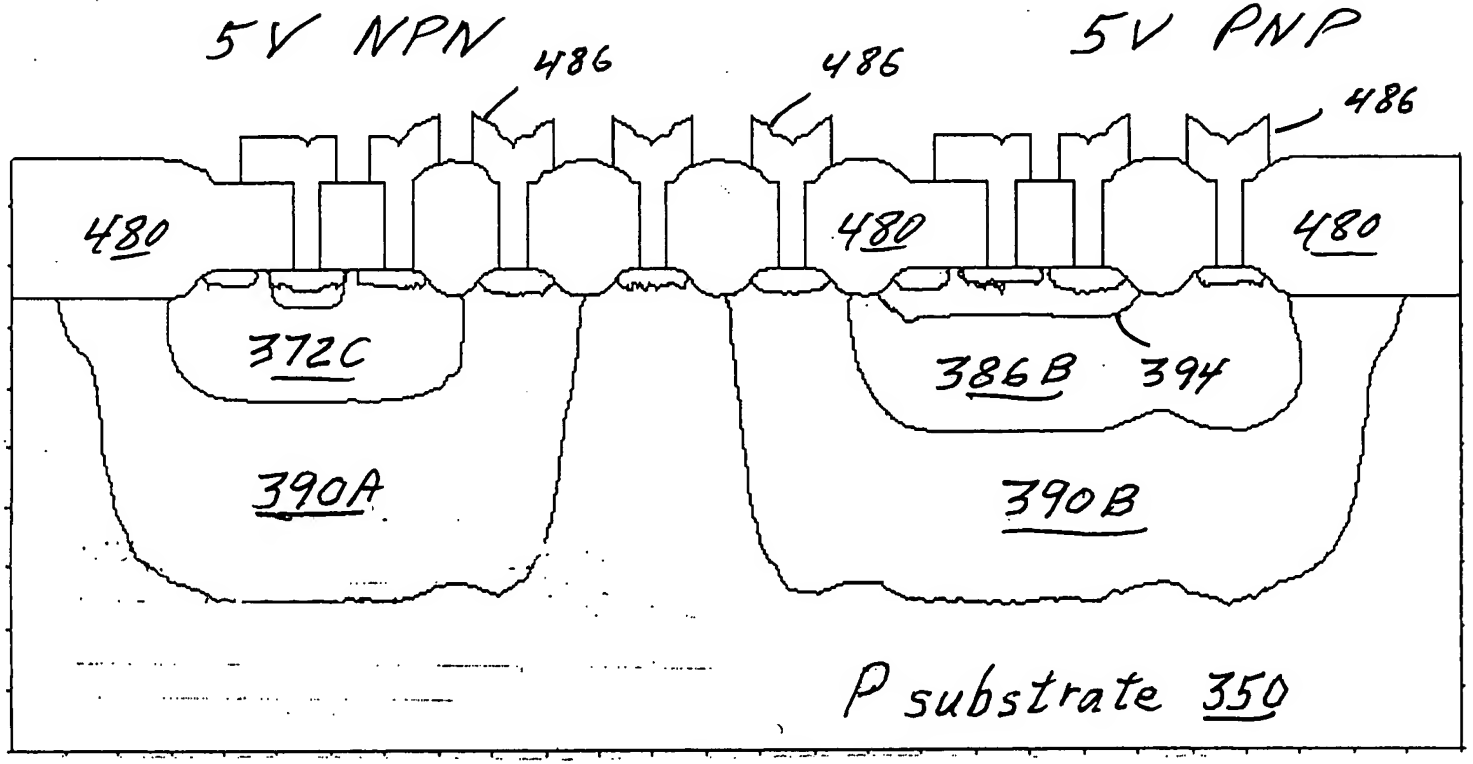


Fig. 67B

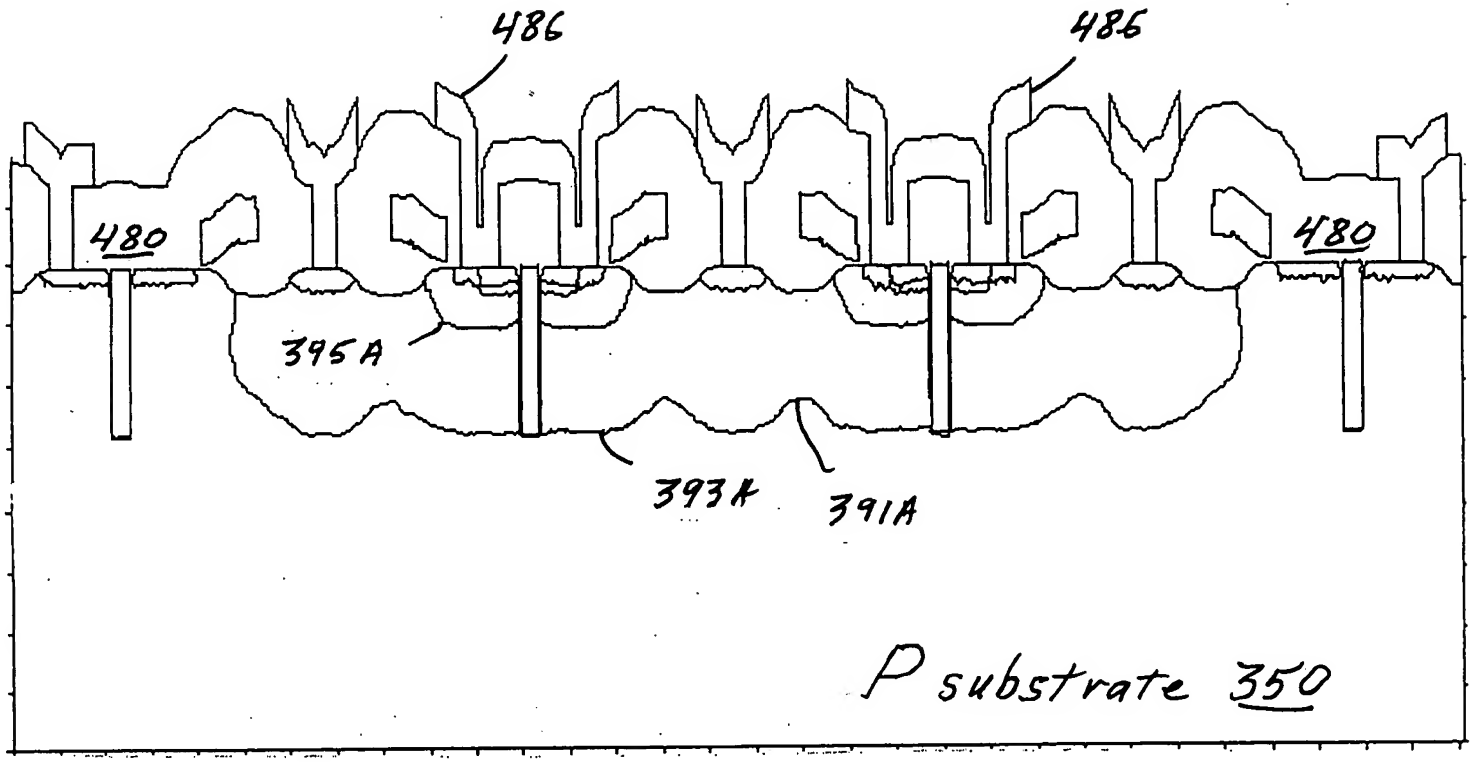
Conventional Layout



Metal Layer

Fig. 67C

30V Lateral Trench DMOS 308

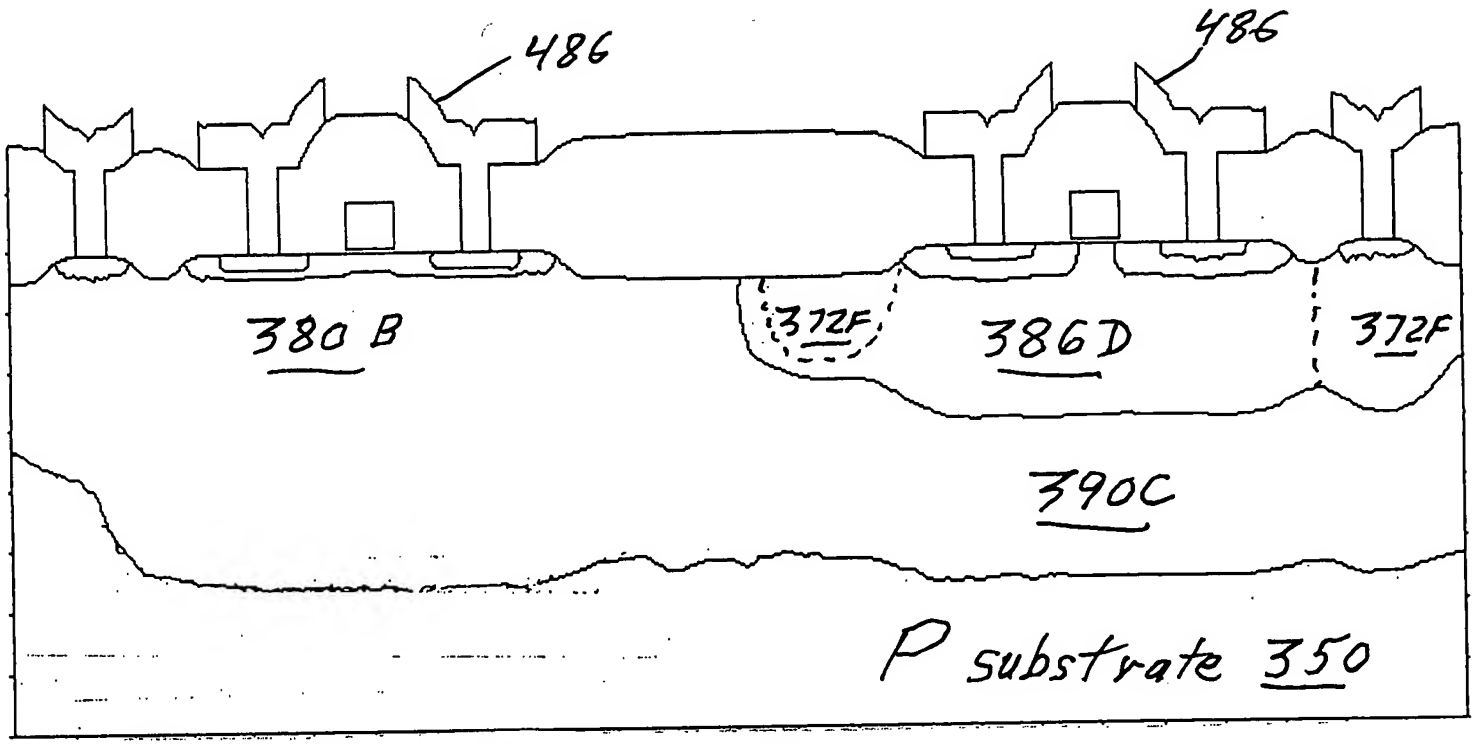


Metal Layer

Fig. 67D

Symmetrical 12V CMOS

12V PMOS 309 12V NMOS 310



Metal Layer

Fig. 6E

Fig. 17V

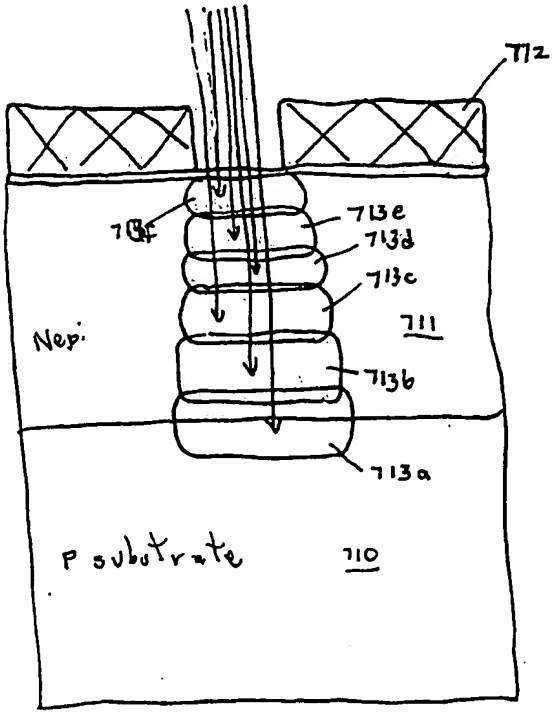


Fig. 17W

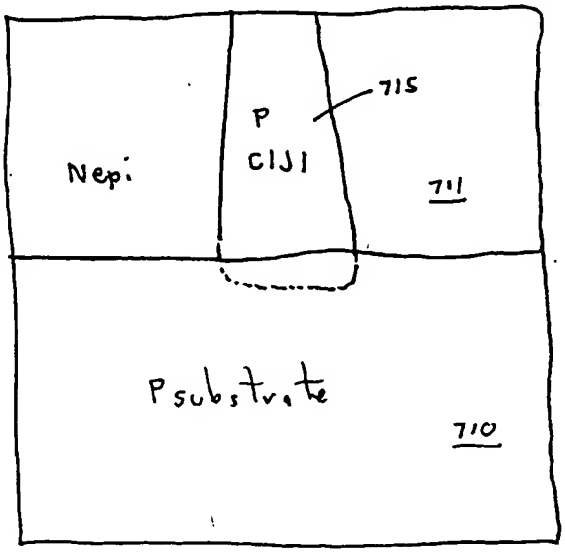


Fig. 17X

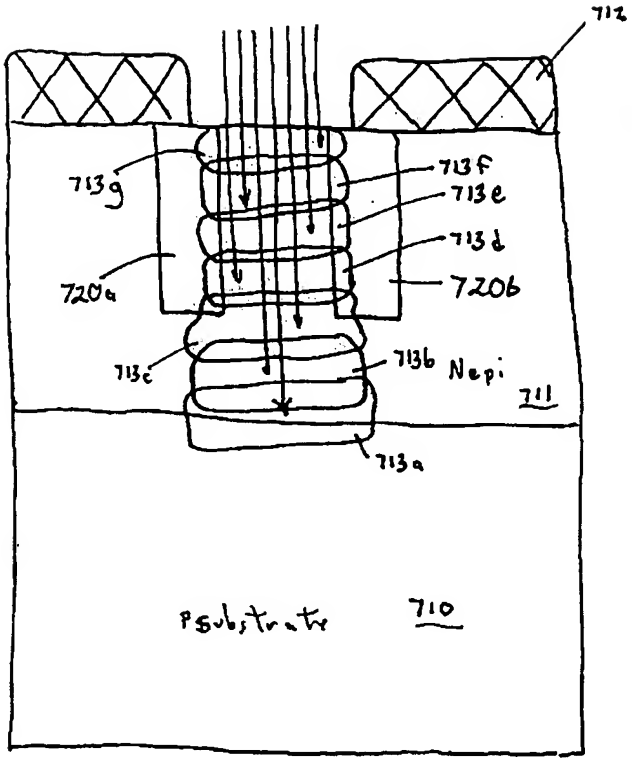


Fig. 17Y

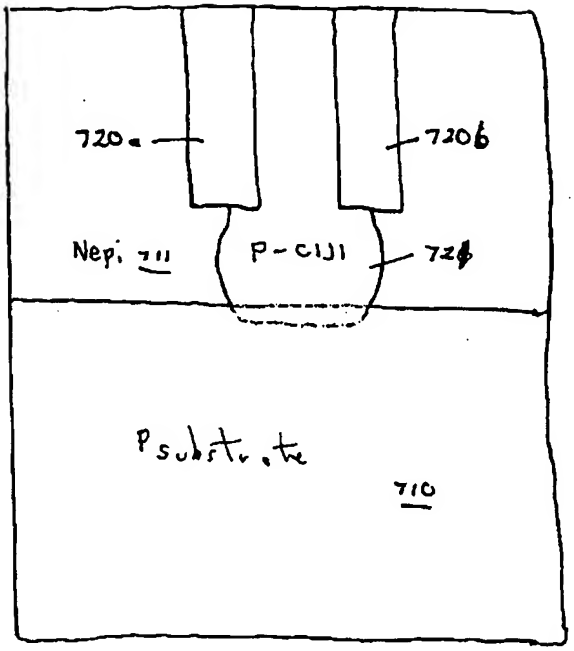


Fig. 17Z

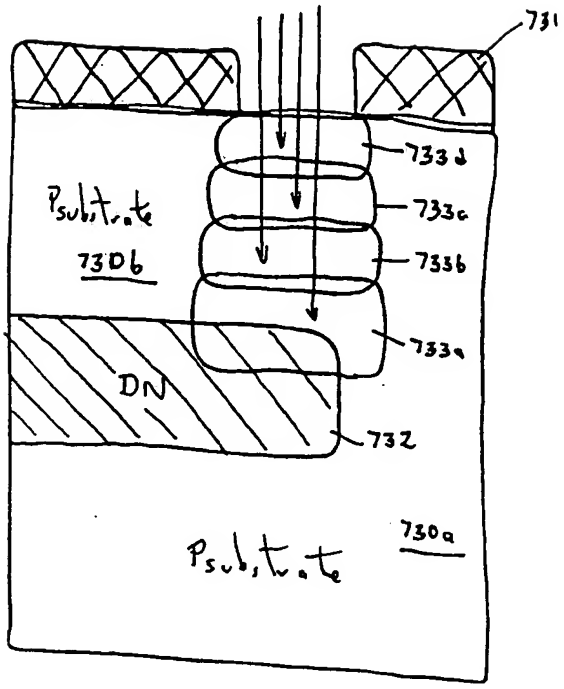


Fig. 17AA

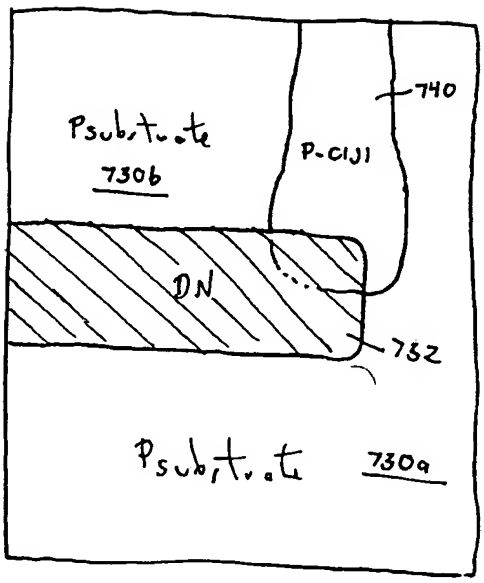


Fig. 17BB

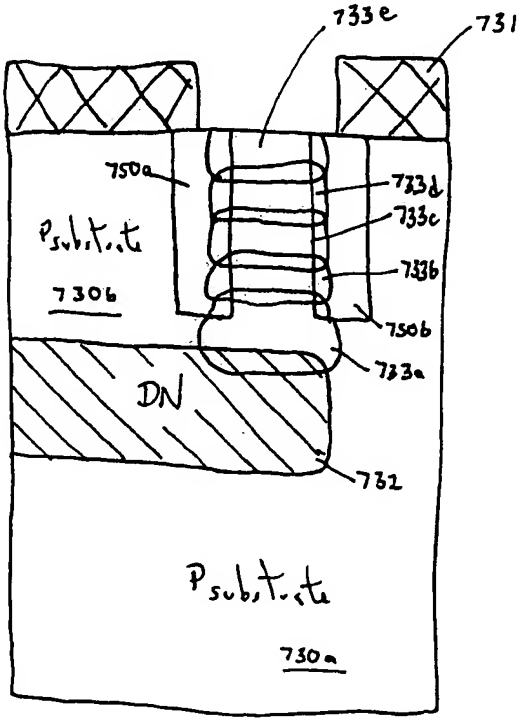


Fig. 17CC

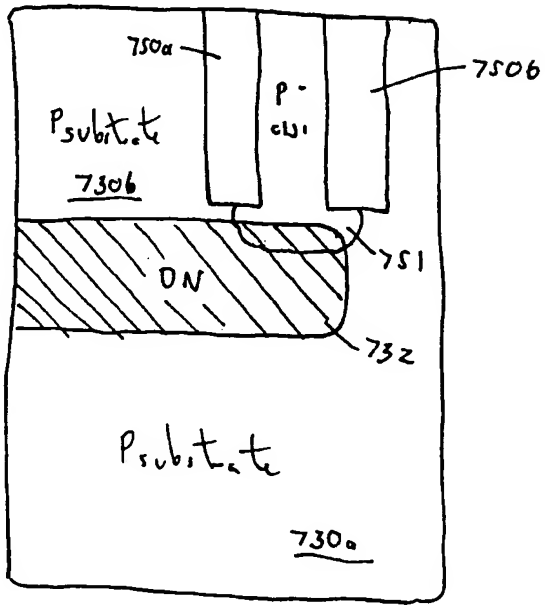
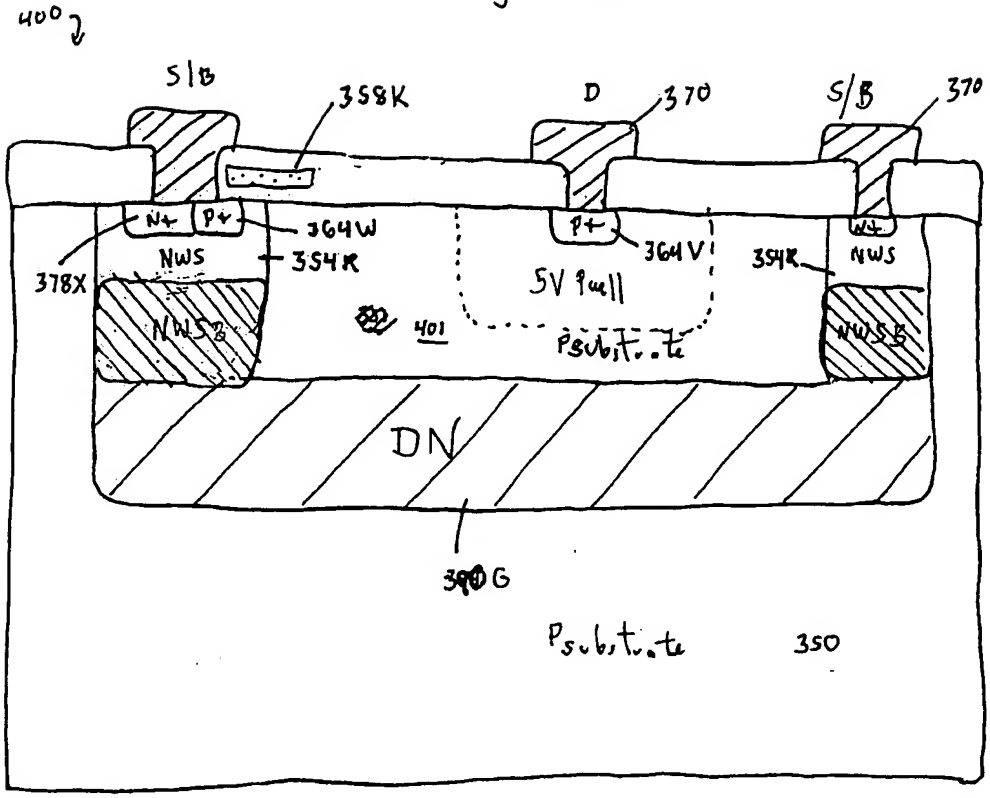


Fig. 18H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S/B
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D
370
S/B
370
N+
P+
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NWS
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5V well
401
Psubstrate
NWSB
NWSB
DN
390G
Psubstrate
350